

1. Circuit description

1.1 Power block

1.1.1 Outline

- (1) The power block is compatible with 100 to 120VAC/220 to 240VAC(50/60Hz).
- (2) The active filter circuit is adopted to suppress the higher harmonic current and improve the power factor.
- (3) The circuit that supplies the electric power to the secondary side is divided into two circuits that are respectively called the main power and sub power.
Though both main and sub circuits supply the power to the secondary side in the normal operation mode, the power is supplied from the sub power only in the power save mode since the main power is stopped.
The main power is the configuration used the flyback converter type switching control IC of the simulative resonant operation. Moreover, the sub power is the configuration used PRC (OFF width fix) control IC.
- (4) The output on the secondary side is shown in Table 1.
(Refer to the power system diagram1-3 in Pages 1-3, 1-4 and 1-5.)

Power block	Output voltage	Application	When power save
Main power side	+215V	H. deflection circuit, Video cut off circuit	OFF
	+80V	Video circuit, DBF circuit, High voltage circuit	OFF
	+15V	H/V deflection circuit, etc.	OFF
	-15V	H/V deflection circuit, etc.	OFF
	+12V	Video circuit, H. deflection circuit, etc.	OFF
	+7.5V	Heater	OFF
Sub power side	+5V	MPU, etc.	ON
	P-OFF+5V	Video circuit, etc.	OFF

Table 1

1.1.2 Rectifying circuit

- (1) The AC input voltage is rectified in the full wave mode with the diode bridge in D901.
- (2) In the higher harmonic circuit of the section 1.1.4, the AC input current becomes the sine wave form in the same phase with the AC input voltage waveform, but the interference is given to other peripheral devices since the noise of the switching current appears on the input side owing to the switching waveform. Therefore, L902 and C906 are inserted to suppress the noise that is caused by the switching current.

1.1.3 Surge current suppression

- (1) TH901 (thermistor) suppresses the rush current that flows when the power switch is turned ON. Moreover, D933 is added to protect D902 from the rush current.

1.1.4 Higher harmonic circuit

- (1) The pulsating waveform rectified in the full wave mode by D901 is switched throughout the full cycle by the frequency of several tens kHz or more. Through this, the input current waveform becomes an average of the switching currents of the partial cycles, thus becoming the sine waveform in the macro. (See Fig.1)
- (2) For the AC input voltage, the AC input current of the sine wave type in the same phase flows to achieve the power circuit of improved power factor and reduced higher harmonic wave component.
- (3) L903 is the choke coil, Q901 is MOS FET, D902 is the rectifying diode, C911 is the block capacitor, and IC901 is the power factor improved controller. The power factor improved controller uses MC33262P of Motorola. (See Fig. 2)
- (4) After the sub power circuit operates, P-SUS signal becomes HI when +5V voltage is supplied to the MPU. Then, Q902 is turned ON, the voltage of approx. +18V is supplied to pin8 (VCC terminal) of IC901 through D929 from pin2 of T902, and the following operation is started.
- (5) The pulsating voltage waveform rectified in the full wave mode by D901 is divided with R904, R905, R906, R907 and R908 (100VAC : 1.1Vp-p and 240VAC: 2.9Vp-p), and is input to pin3 of IC901 (Multiplier input). Moreover, the output (+side of C911: 400VDC) of the higher harmonic circuit is divided with R913, R914, R915, R916 and R917 (2.5VDC), and is input to pin1 of IC901 (error amplifier input).
- (6) The output of the error amplifier and the divided waveform of the pulsating voltage input to pin3 of IC901 sets the threshold voltage of the current sense comparator to control the Q901 flowing current from zero to the peak line of the AC input voltage in the sine wave pattern.
- (7) When Q901 is turned ON, the drain current of Q901 flows to R910 and R937 to drop the voltage, and the voltage generated by the voltage drop is input to pin4 (current sense input) of IC901. When the voltage reaches the threshold voltage of the current sense comparator, Q901 is turned OFF.
- (8) When Q901 is turned OFF, the accumulated energy of L903 starts to be supplied to the load through D902.
- (9) As the accumulated energy of L903 drops, the auxiliary coil voltage (pin8 of L903) also drops. When it reaches the threshold voltage of *zero current detector, Q901 will be turned ON again.
 - * Pin 5 of IC901 is the zero current detection terminal to input the auxiliary coil voltage of pin10 of L903. The zero current detector monitors that the auxiliary coil voltage drops beyond the threshold voltage. Thus, the accumulated energy of L903 is indirectly detected.
- (10) The above operation is repeated to continue the oscillating operation. Thus, the DC voltage (L903, Q901, D902 and C911 compose the voltage rise circuit.) is gained on the output, and the AC input current of the sine wave in the same phase with the AC input voltage is gained on the input side.

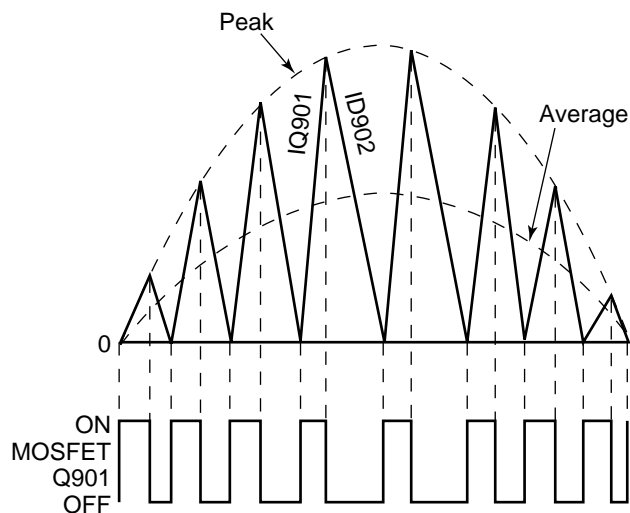


Figure 1. L903 coil current

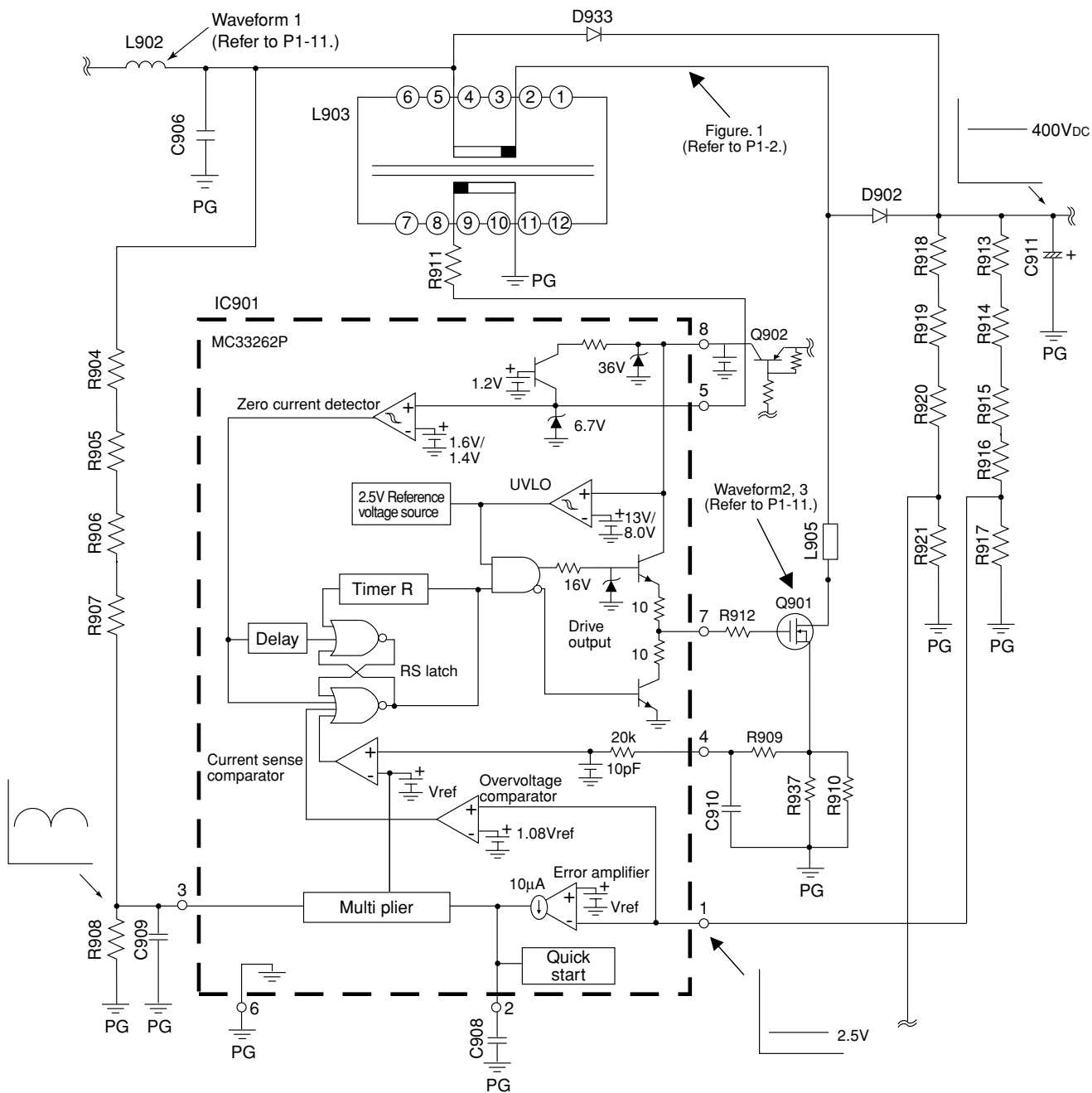


Figure 2. High harmonic waveform circuit

1.1.5 Sub power circuit

- (1) The sub power uses PRC control regulator STR-G6352 (IC903) produced by Sanken Electric. (See Fig.3)
- (2) When the power switch is turned ON, the rectified and smoothened DC voltage (AC voltage $\times \sqrt{2}$) is supplied to pin4 of IC903, through R950, R951 and R952. When pin4 reaches approx. 17V, the built-in output FET is put into operation. (Since Q902 is OFF, IC902 and IC 903 do not operate.)
- (3) This also induces the voltage at pin2 of T902 and on the secondary side. These outputs are respectively rectified, and are used as the power for control on the primary side and the power for the MPU.
- (4) IC903 monitors +5V and -15V output on the secondary side by IC922 (Shunt regulator), and suppresses the voltage regulation by feeding back to pin 5 of IC903 via IC912 (Photocoupler).
- (5) When the voltage on the secondary side starts, the MPU will be put into operation and the P-SUS signal line will become HIGH.
- (6) This information is transmitted to the primary side via IC913 to turn ON Q902.
When Q902 is turned ON, the power for control on the primary side will be supplied to IC901 and IC902 to operate the higher harmonic circuit. Thus, the main power circuit will be put into operation.

1.1.6 Main power circuit

- (1) The main power circuit adopts the flyback type switching power of pseudo-reonance operation. This is composed of a Sanken brand hybrid IC STR-F6676 (IC902) that integrates the power MOS-FET and control IC.
The circuit operation is described as follows. (See Fig. 4.)
- (2) The timing at that the power MOS-FET is turned ON is consistent with the bottom point of the voltage resonant waveform after the transformer (T901) discharges the energy to the secondary side, that is, a half cycle of the resonant frequency determined by LP value (primary coil inductor value) of T901, and C914 (resonant capacitor). This is called pseudo-reonance operation. The advantage of such an effect is that the switching loss is reduced by turning it ON when the voltage between the drain sources of the power MOS-FET becomes the lowest.
- (3) Like the higher harmonic circuit, voltage of approx. +18V is supplied to the Vcc terminal (Pin 4) of IC902 (STR-F6676) via D929 from pin2 of T902 when Q902 is turned ON by the P-SUS signal from the MPU.
When the voltage of Pin 4 of IC902 reaches 16V, the control circuit will be put into operation to turn ON the integrated MOS-FET.
- (4) When MOS-FET is turned ON, the capacitor C1 in IC will be charged to approx. 6.5V. On the other hand, the drain current flows to R928, and the voltage generated by the voltage drop is applied to pin1 (OCP/FB terminal) of IC902.
When the voltage of Pin 1 reaches approx. 0.73V, the comparator (Comp. 1) in IC will be activated to turn OFF MOS-FET.
- (5) The voltage between both ends of C1 drops to approx. 3.7V. the oscillator output will be reversed again to turn ON MOS-FET.
The above is repeated to continue the oscillation operation.
- (6) Here, IC902 monitors +215V of the output on the secondary side with IC921 (error amplifier) and feeds back it to pin1 of IC902 via IC911 (photocoupler), thus suppressing the voltage fluctuation of the primary side.

Figure 3. IC903 (STR-G6352) block diagram and peripheral circuit

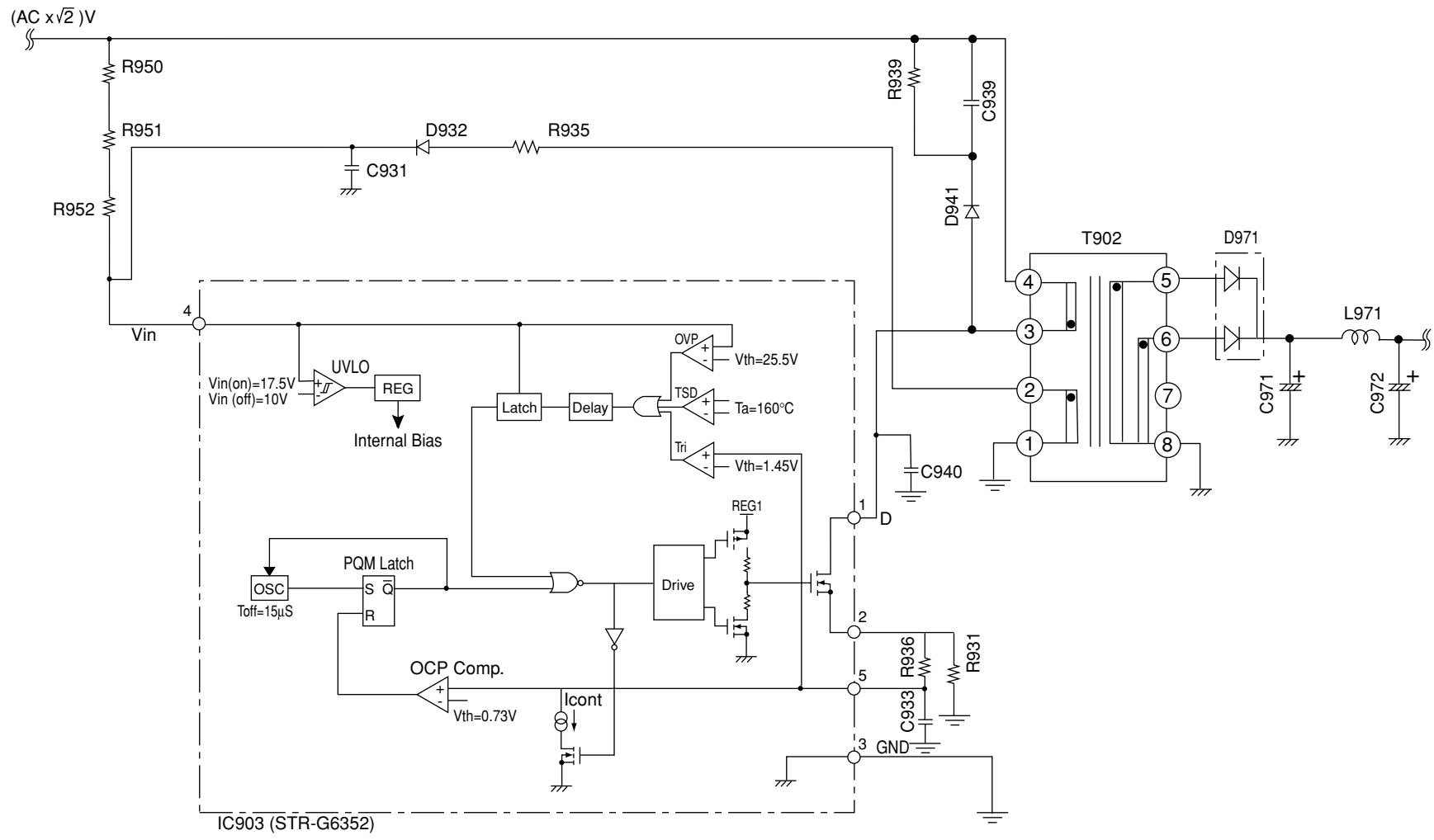
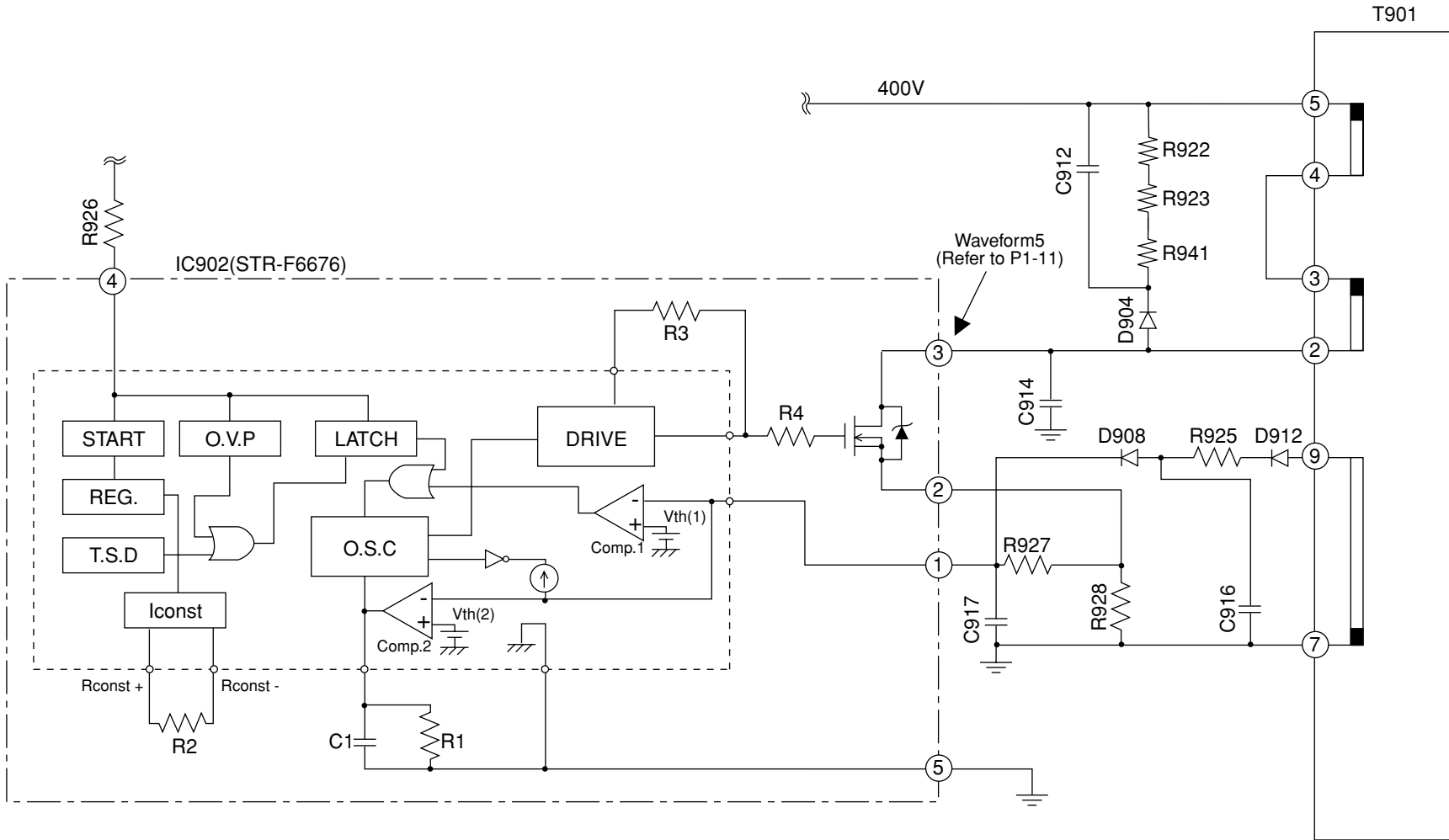


Figure 4. IC902 (STR-F6676) block diagram and peripheral circuit



1.1.7 Degaussing circuit

- (1) The automatic and manual degaussing circuit is provided.

The circuit prevents the picture from dropping its quality due to the magnetization on CRT, and operates as follows.

- (2) When powering ON, Q963 flows to activate RY901 by DG signal output by the MPU.

This will make the current flow through the demagnetizing coil for demagnetization. The demagnetizing time is approximately 5 seconds.

Manual demagnetization becomes possible by selecting the demagnetizing menu on the OSD picture.

1.1.8 Power management circuit

Turn ON the power management setting on the menu picture of OSD, and the energy saving mode shown in Table 2 will be ready depending on whether the horizontal/vertical sync. signal is present or not.

Power Save	H-sync	V-sync	Video	Power consumption	Recovery time	Power-On Indicator
OFF	On	On	Active	140W		Green
ON	Off	On	Blank	3W	5 sec.	Orange
	On	Off	Blank			
	Off	Off	Blank			

1.1.9 Protective circuit

- (1) Overcurrent protective circuit (primary side)

IC902 is provided with an overcurrent protective circuit. The voltage drop generated by the drain current that flows into R928 is input to Pin 1 (OCP/FB terminal) of IC902. When the voltage reaches 0.73V, the overcurrent protective circuit will be activated.

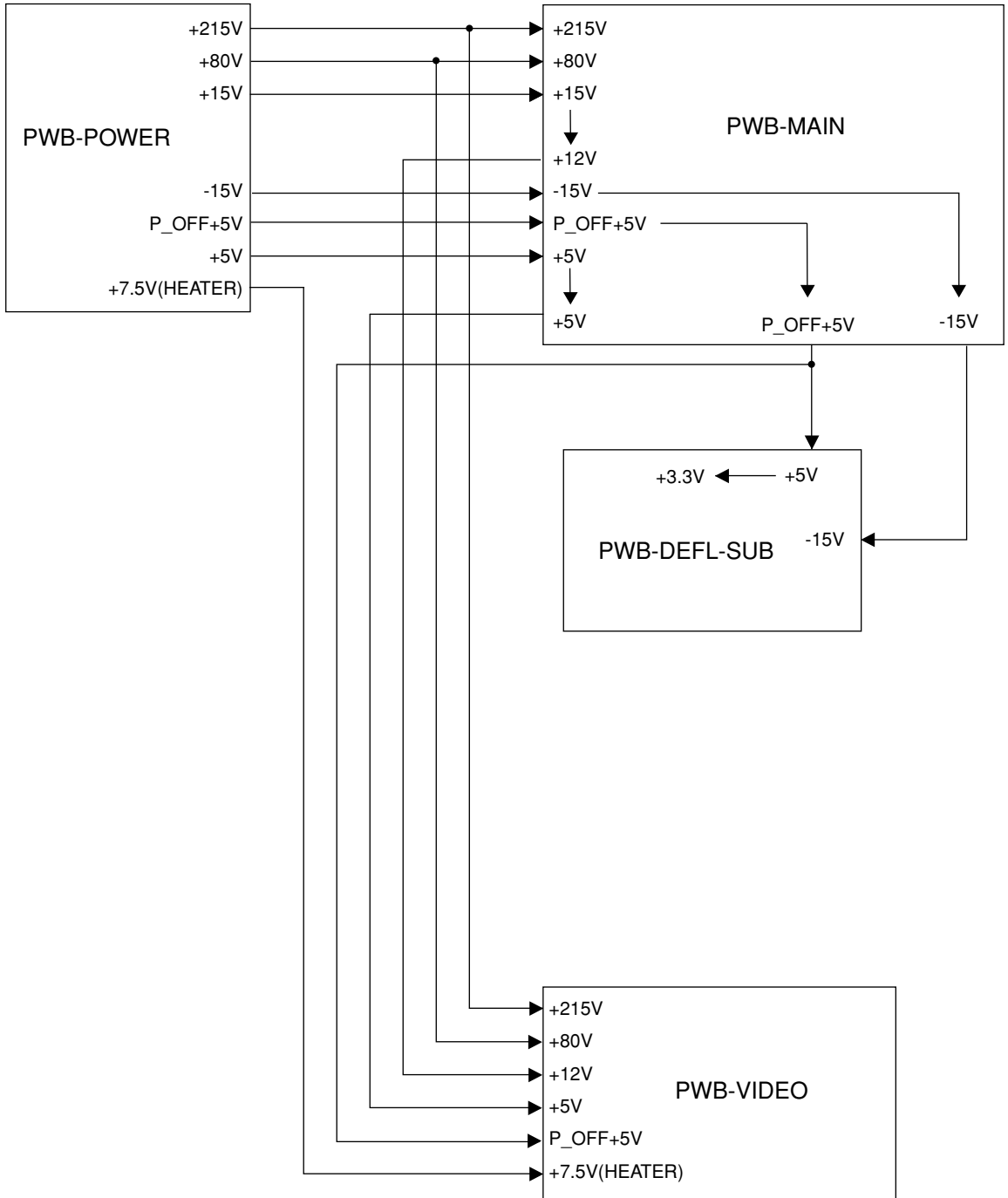
- (2) Overcurrent protective circuit (secondary side)

To protect the parts on the secondary side, the short-circuit detection circuit is provided on the secondary side output (+215V, +80V, +/-15V, +7.5V), one for each. As an example of +215V, the output line of +215V is monitored with R964, R965, D966 and Q961. If it drops beyond approx. +140V for any reason, Q961 will be turned ON to transmit the information to the MPU. Then, since the MPU sets P-SUS signal at LOW, Q902 will be turned OFF to cut off the power to IC902 in order to stop IC902. (IC901 will be also stopped at the same time.) The overcurrent protective circuit is designed to be activated when the output voltage drops approx. 30 to 40%.

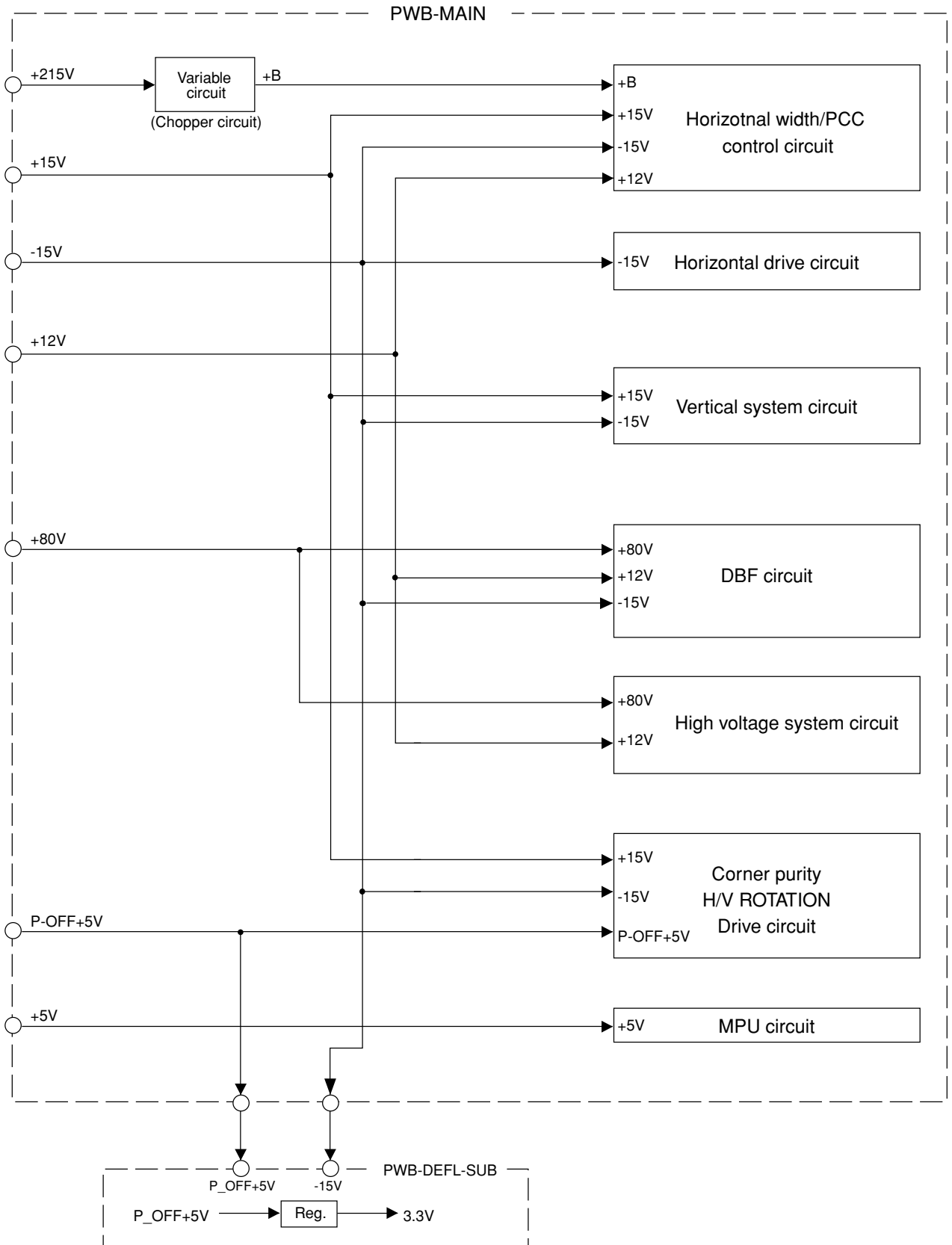
- (3) Overvoltage protective circuit

R918, R919, R920 and R921 are used to detect the overvoltage in the higher harmonic circuit, and the tertiary coil (Pin 9) of T901 is used to detect the overvoltage of the voltage on the secondary side. They are both connected to the overvoltage protective circuit (Q904, Q905) on the primary side. If any overvoltage results for any reason, Q905 will be turned ON to turn ON Q904. Then Q902 will be stopped. Since the power for IC901 and IC902 is cut off as Q902 is stopped, the switching operation will be stopped.

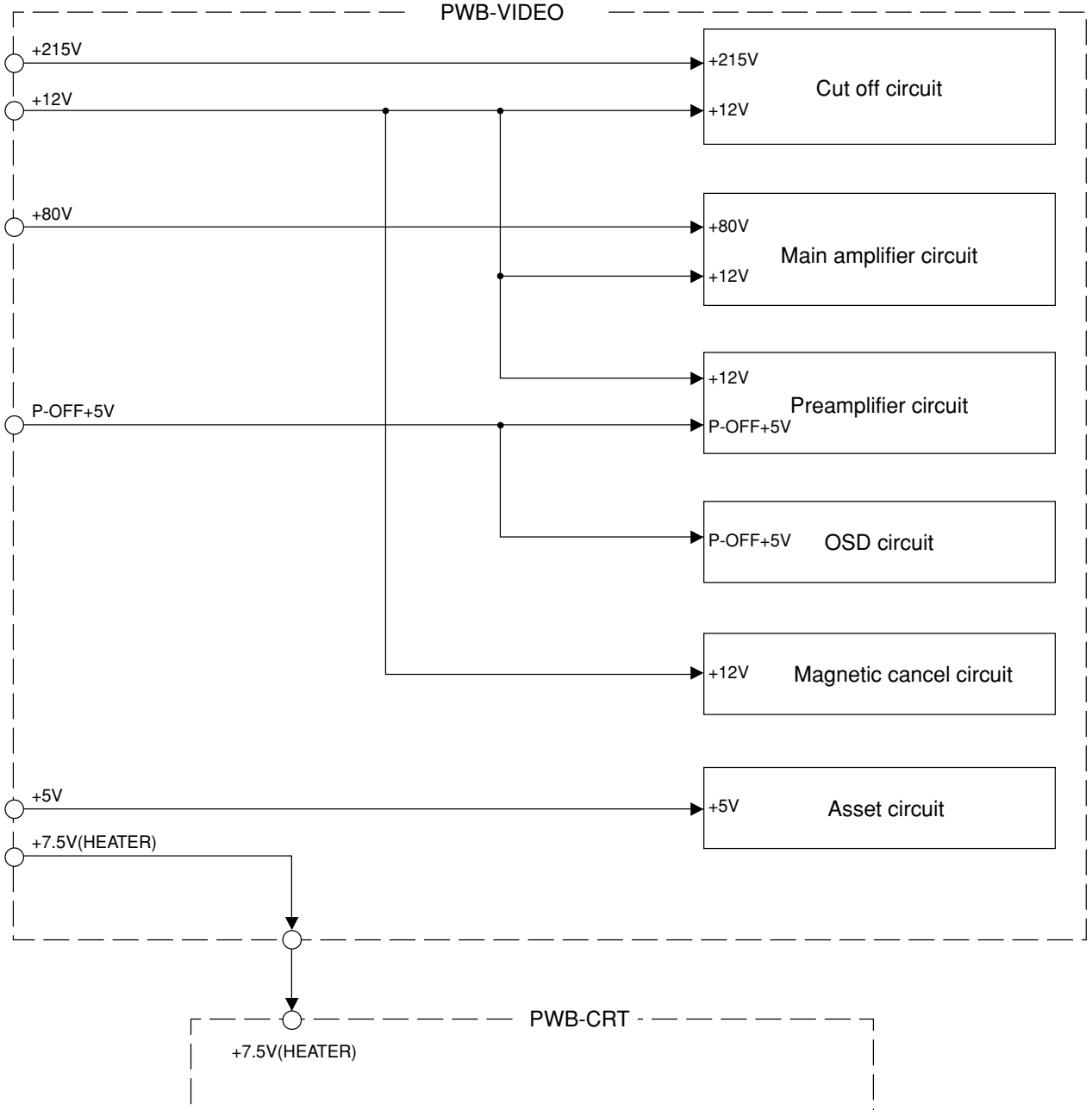
~ Power system diagram 1 ~

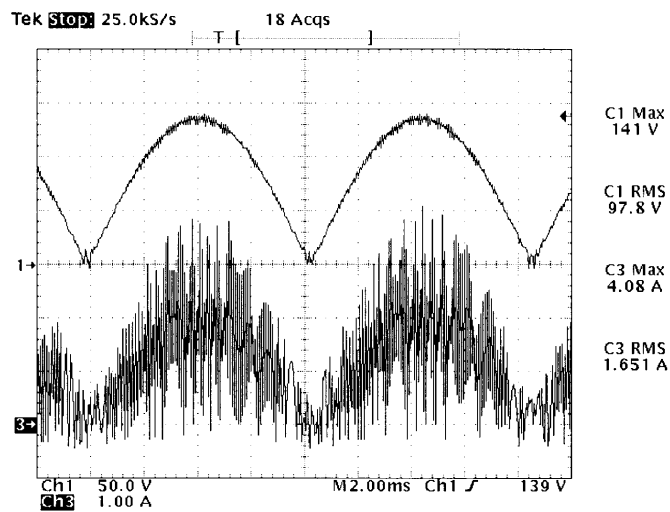


~ Power system diagram 2 ~

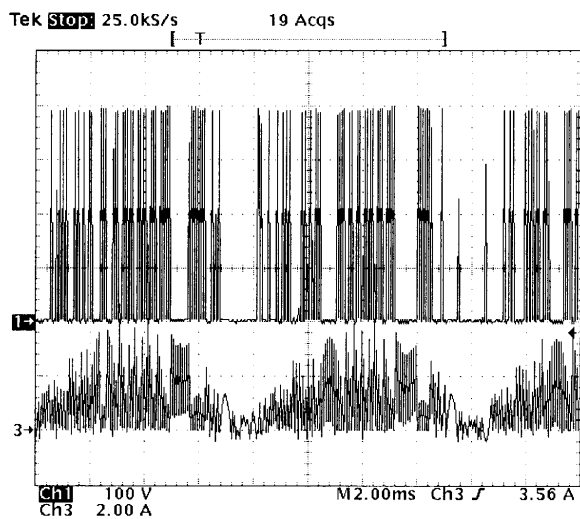


~ Power system diagram 3 ~

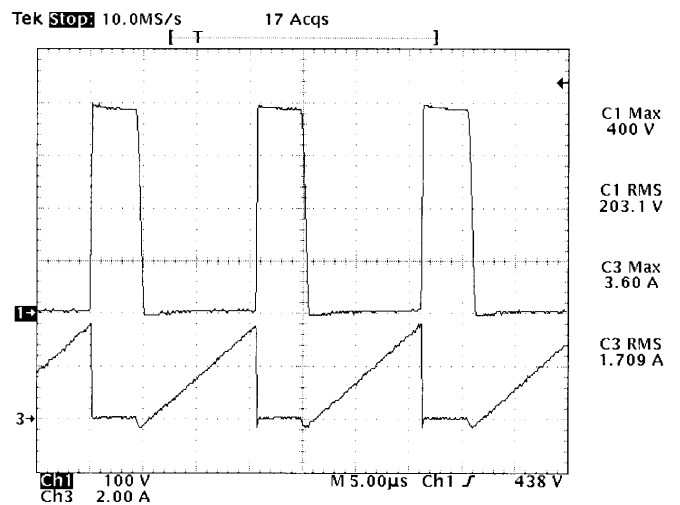




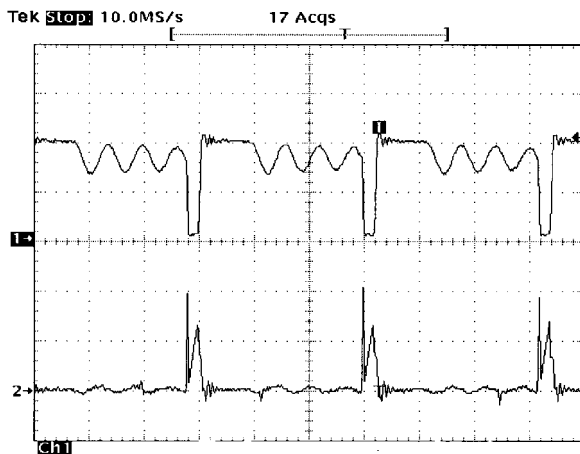
Waveform 1. Top :AC input voltage
Bottom :AC input current



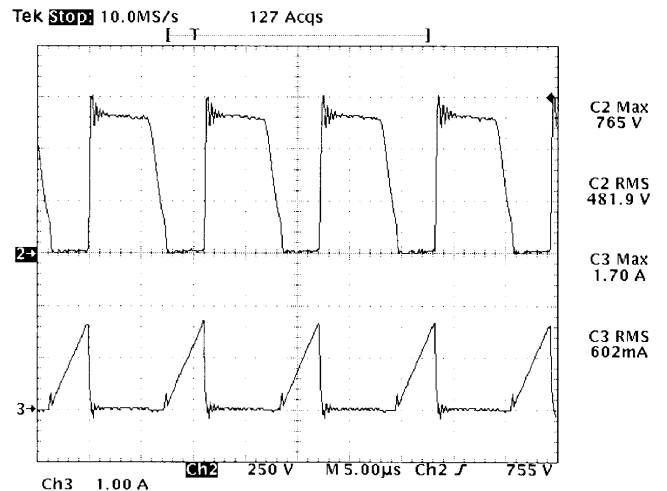
Waveform 2. Top :Q901 drain voltage
Bottom :Q901 drain current



Waveform 3. Top :Q901 drain voltage
Bottom :Q901 drain current



Waveform 4. Top :IC903 drain voltage
Bottom :IC903 drain current



Waveform 5. Top :IC902 drain voltage
Bottom :IC902 drain current

1.2 Horizontal deflection block

The operating principle of the horizontal deflection circuit is given below.

The Q502 operates as horizontal output, and the D503 as the dumper diode.

As shown in Fig. 5, the horizontal output transistor Q502 turns to ON/OFF by means of the drive pulse in pin 25 of IC601 in substrate DEFL-SUB through the drive transformer T501, drive transistor Q501, or Q560, Q561, Q562, etc.

The deflection current I_{dy} during Q502 ON gets increased to the maximum level I_p according to the equation shown below:

$$I_{dy} = (V_{cc}/L_{dy}) \times T_{on}$$

The maximum I_p is approximately 8A at full scan when $f_h = 106k$.

Here;

V_{cc} : Output voltage of Q504

L_{dy} : Parallel value of the L_h value of DY (=62 μ H) and the horizontal output transformer (=5mH)

T_{ON} : The ON time of Q502

When the drive pulse has negative polarity, Q502 turns OFF and I_{dy} starts flowing to charge C506 until the collector voltage reaches the maximum level V_{cp} .

$$V_{cp} = V_{ccx}\{1 + (\pi/2) \times (T_s/T_r)\}$$

With the maximum V_{cp} attained, the charges accumulated in C506 flow into DY as the discharge current. This charge/discharge current is called retrace time, and is expressed by the equation given below.

$$T_r = \pi\sqrt{L_{dy} \cdot C_r} \quad * C_r = C506 \text{ value}$$

In the present model, the retrace time is set to approx. 1.8 μ s.

T_s is called trace time, and is expressed by the equation given below with the horizontal cycle as T.

$$T = T_s + T_r$$

With $V_{cp} = 0$, the dumper diode D503 turns ON and I_{dy} gets decreased from $-I_p$ to 0 ampere. Since Q502 ON time and dumper diode ON time are set to overlap at 0 ampere point of I_{dy} , the crossover distortion is prevented from occurring at 0 ampere point of I_{dy} .

The D503 causes the transient current to flow in the high-speed dumper diode.

The horizontal output transformer T502, connected in parallel to the deflection yoke, operates as a choke coil. Figs. 6 and 7 show the image of circuit operation and the waveforms in actual machine.

1.2.1 Distortion compensation waveform generating circuit

The deflection distortion compensation waveform for horizontal size system is output from pin 64 of IC601. This waveform is output from 1-bit DAC, with 3.3V pulse waveform with resolution 25MHz output at pin 64. This pulse waveform is leveled by the low-pass filters R632 and C622 to obtain the vertical cycle compensation waveform, with the amplitude 1.0 to 1.2Vp-p and connected to pin5 of IC5J1.

The compensation waveform circuit carries out horizontal size and trapezoid compensation, side pin compensation, side pin top and bottom compensation, side pin S-shape compensation and side pin W compensation. (Refer to Compensation Image Diagram in Fig. 22)

The deflection compensation waveform for horizontal phase system is output from pin 57 of IC601. The pin 57 has 1-bit DAC output and outputs the 3.3V pulse waveform with 25MHz resolution. This pulse waveform is then leveled by the low-pass filters R619, R614, C604 and C601 to obtain the vertical cycle waveform, which is then electrically added to the horizontal system PLL filter (pin 20 of IC601) to carry out the deflection distortion compensation of the horizontal phase system. It carries out parallelogram distortion compensation and side pin balance (top and bottom) correction. (Refer to the Compensation Image Diagram in Fig. 22.)

The control of horizontal screen width and the side PCC control are carried out by IC5J1, Q503 and Q504. First, the horizontal width signal and each distortion compensation signal impressed in pin 5 of IC5J1 from pin 64 of IC601 are compared with the AFC pulse signal rectified and fed back to pin 13 of IC5J1. The signals are further compared with the constant-inclination type saw-tooth wave synchronized with the horizontal cycle created inside IC before turning into the PWM signal of square wave. This PWM signal output from pin 9 of IC5J1 carries out the above control by driving the Q504 gate. Fig. 8 shows the block diagram of IC5J1 and Fig. 9 the operation image waveforms.

IC5K1 connected to pin 8 of IC5J1 is a transistor with 2 circuits.

Pins 1 and 3 of IC5K1 are for the base, pin 2 is for GND and pins 4 and 5 are for the collector.

Pin 32 of IC101 connected to pin 3 makes pins 5 and 2 open/short by P-SUS signal.

When P-SUS signal is LOW, pin 8 of IC5J1 is led into GND from pin 5 of IC5K1, and make SYNC input of IC5J1 LOW. As IC5J1 stops operation without SYNC input, Q504 turns OFF and horizontal deflecting output stops.

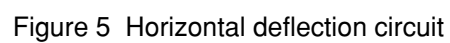
Due to this process, destruction by wrong pulse is prevented when it exceeds in Q502.

The Q503 works as a ripple filter in 215V line and keeps the Q503 emitter voltage constant even if there is a slight fluctuation in the collector voltage of Q503. The Q503 collector has 215V applied to it, with the emitter output being stable at 203V. This is mainly effective in dynamic regulation.

The horizontal raster position is adjusted by using Q5A1, Q5A2, VR5A1 and T502. The reference voltage is obtained from the connecting point of Cs and is then input into pin 2 of T502. When the emitter voltage in Q5A1 and Q5A2 has the DC level increased by adjusting VR5A1, the current flows to DY side, causing the raster to move left. Reversely, when the DC level of the emitter voltage is decreased, the current flows to Q5A2 side, causing the raster to move right.

The Idy DC level is adjusted by varying the emitter voltage of Q5A1 and Q5A2 at the timing No. 25 (120kHz/85Hz) using VR5A1, so that the raster position comes at the center of CRT. The operation image is shown in Fig. 10.

This adjustment, however, is confined to the factory, and is not open to the users.



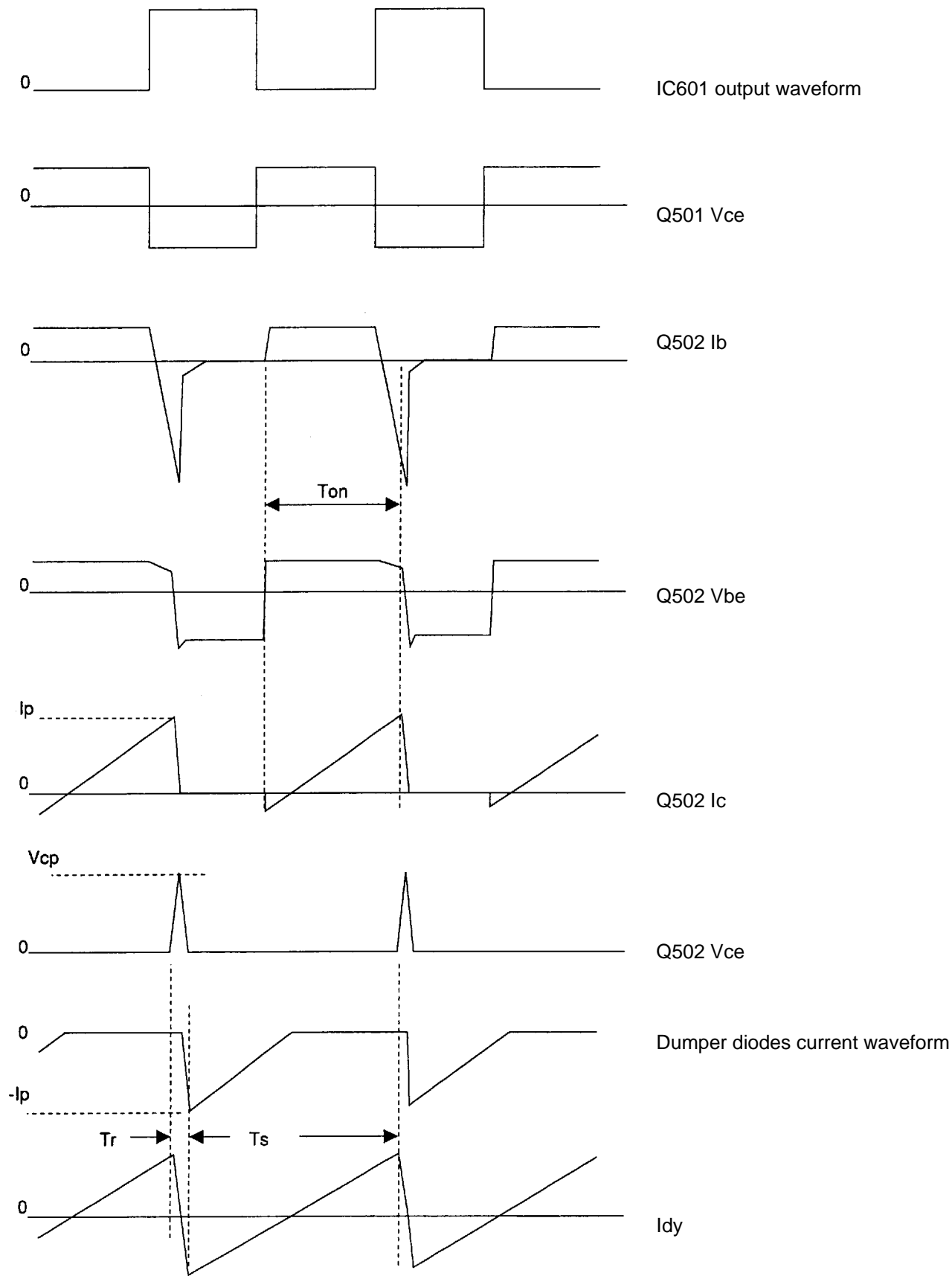
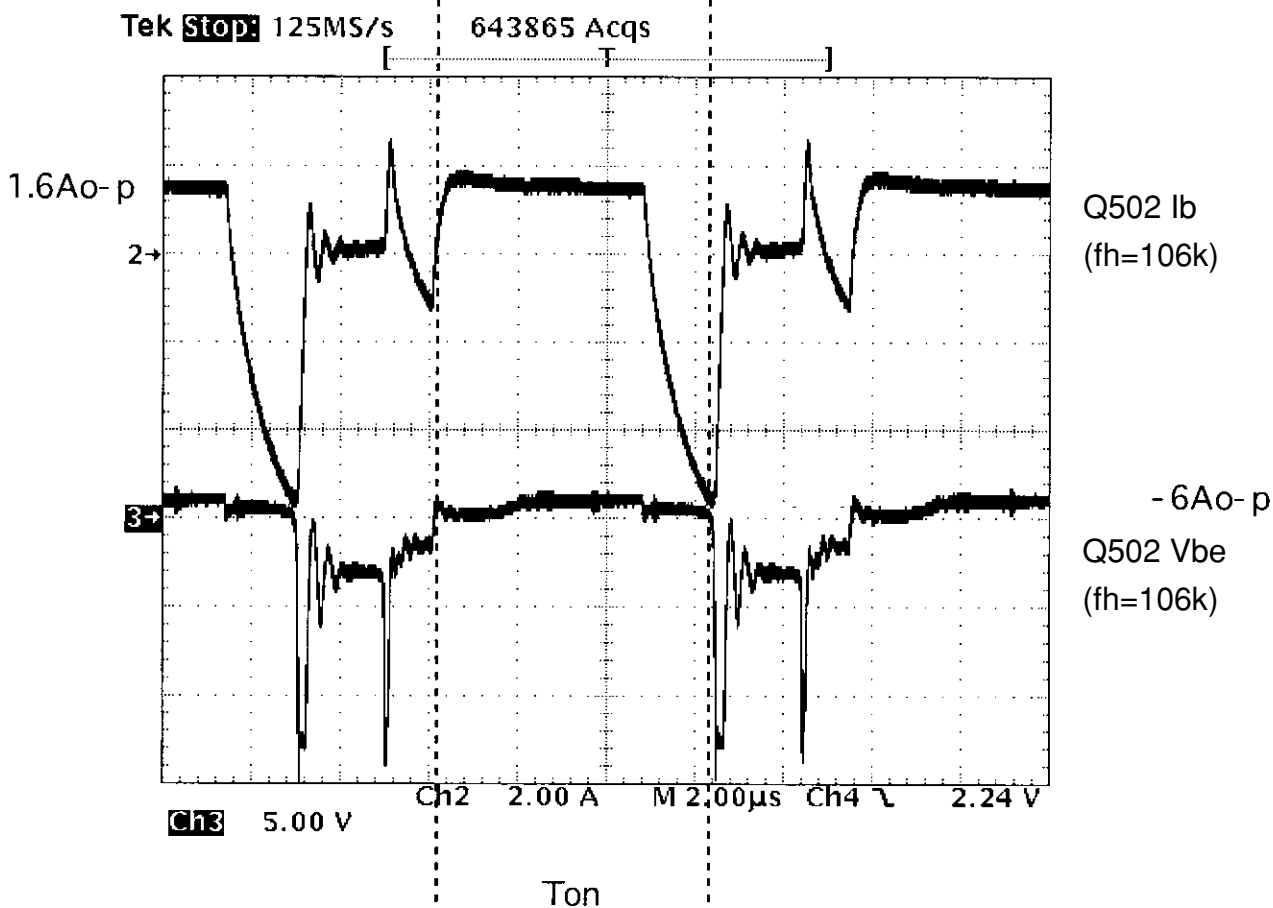
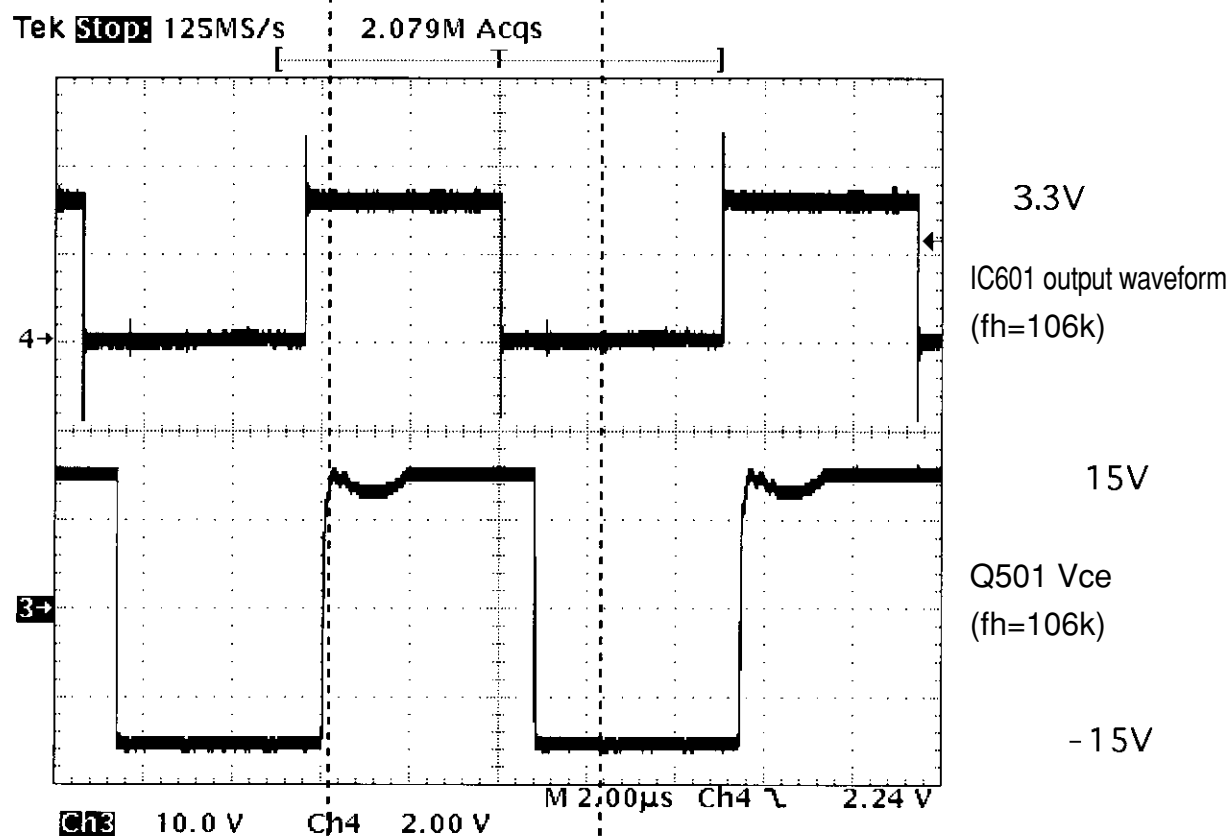


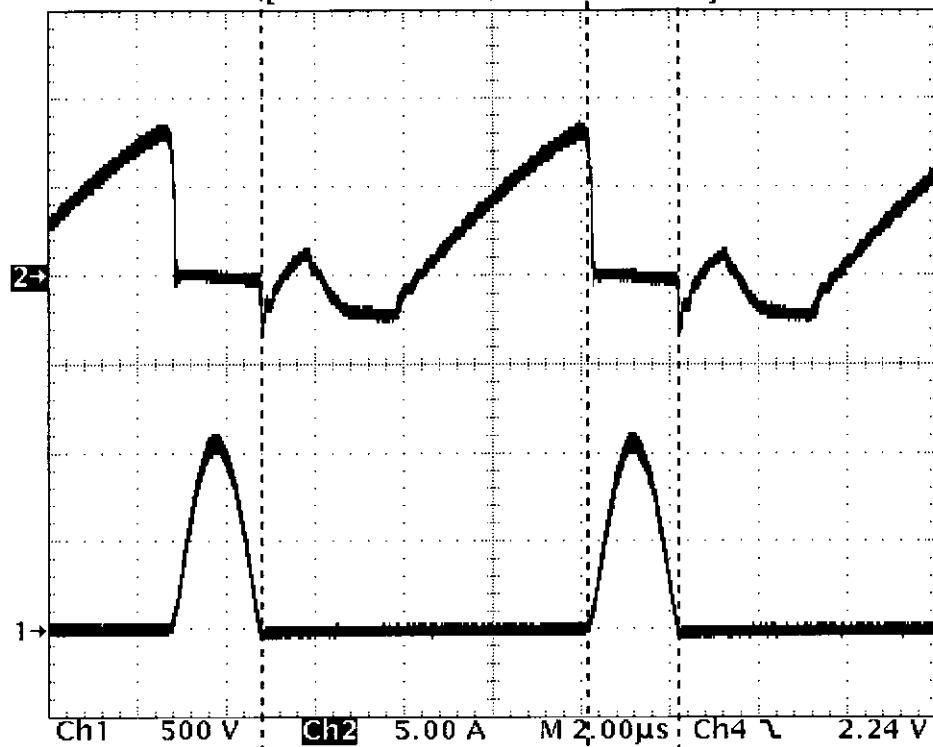
Figure 6 Horizontal deflection circuit operation image

Figure 7. Deflection circuit waveform while fh=106k



Tek Stop: 125MS/s

45704 Acqs



8Ao-p

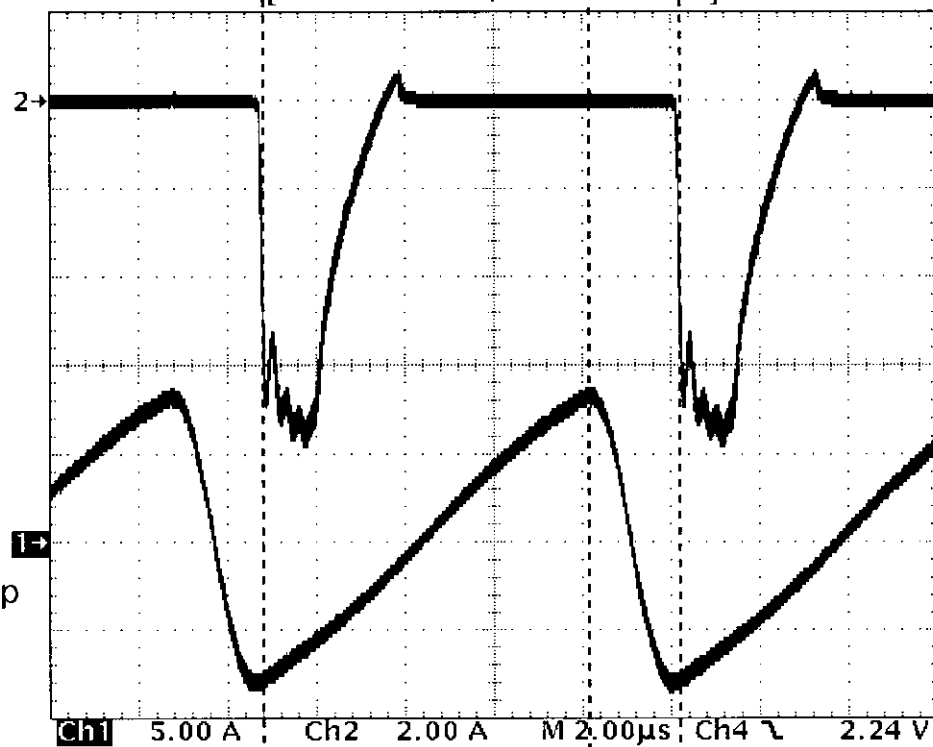
Q502 I_c
(fh=106k)

1100Vp

Q502 V_{ce}
(fh=106k)

Tek Stop: 125MS/s

357860 Acqs



Damper diode
Current waveform
(fh=106k)

-7.5Ao-p

I_{dy}
(fh=106k)

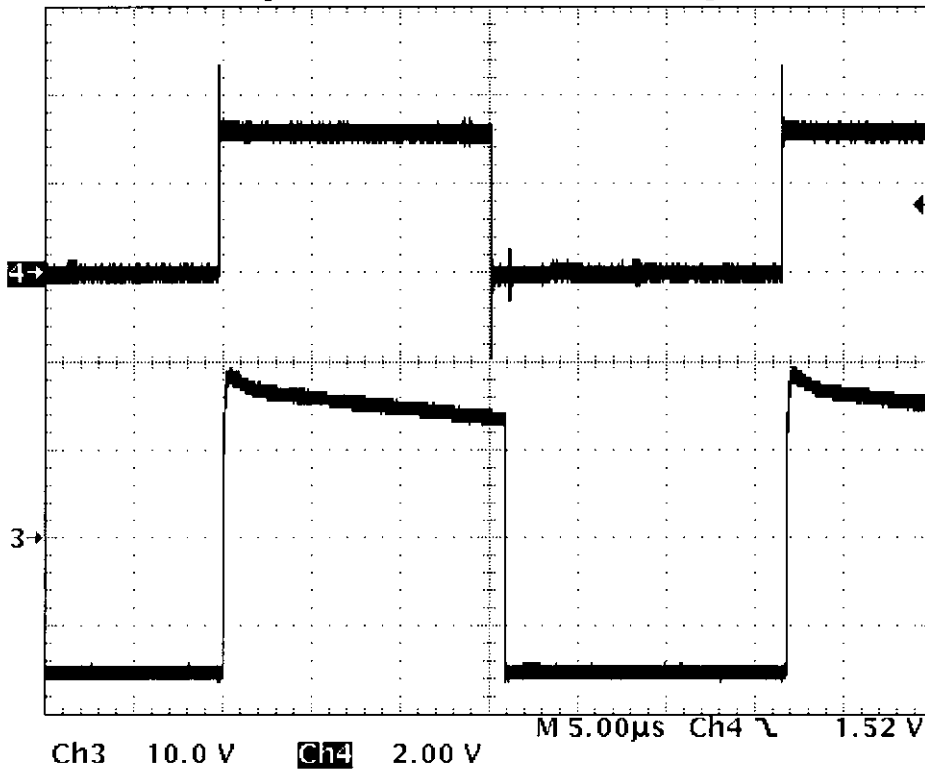
16Ap-p

T_s

T_r

Deflection circuit waveform while fh=31.5k

Tek **Stop:** 100MS/s 9506 Acqs DPO Brightness: 20 %



3.3V

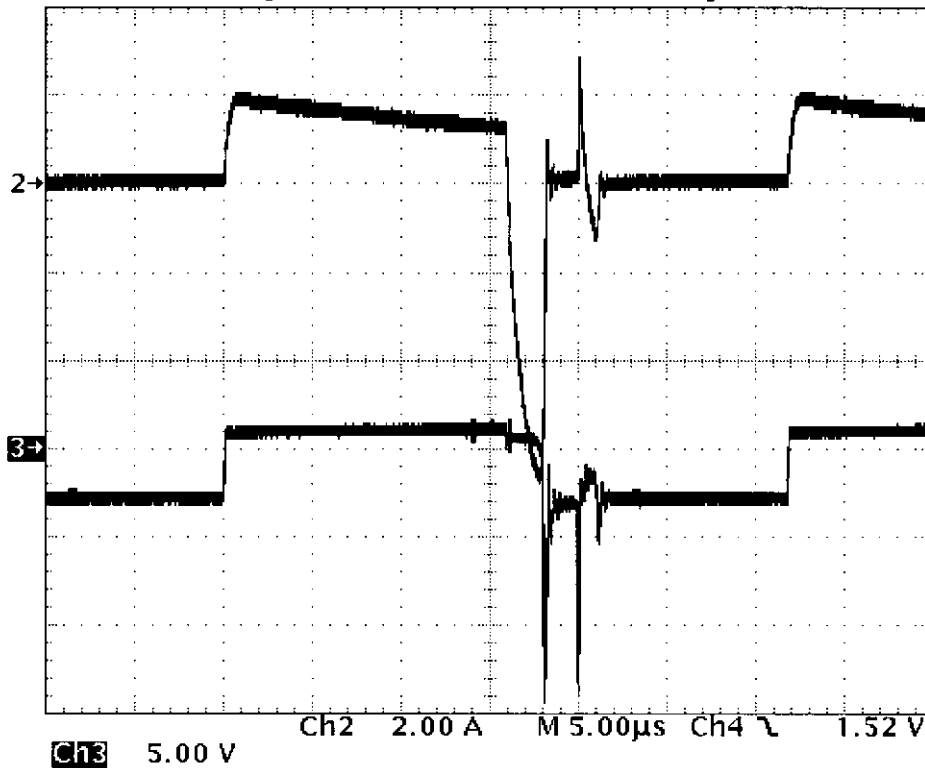
IC601 output waveform
(fh=31.5k)

20V

Q501 Vce
(fh=31.5k)

-15V

Tek **Stop:** 100MS/s 74864 Acqs DPO Brightness: 20 %

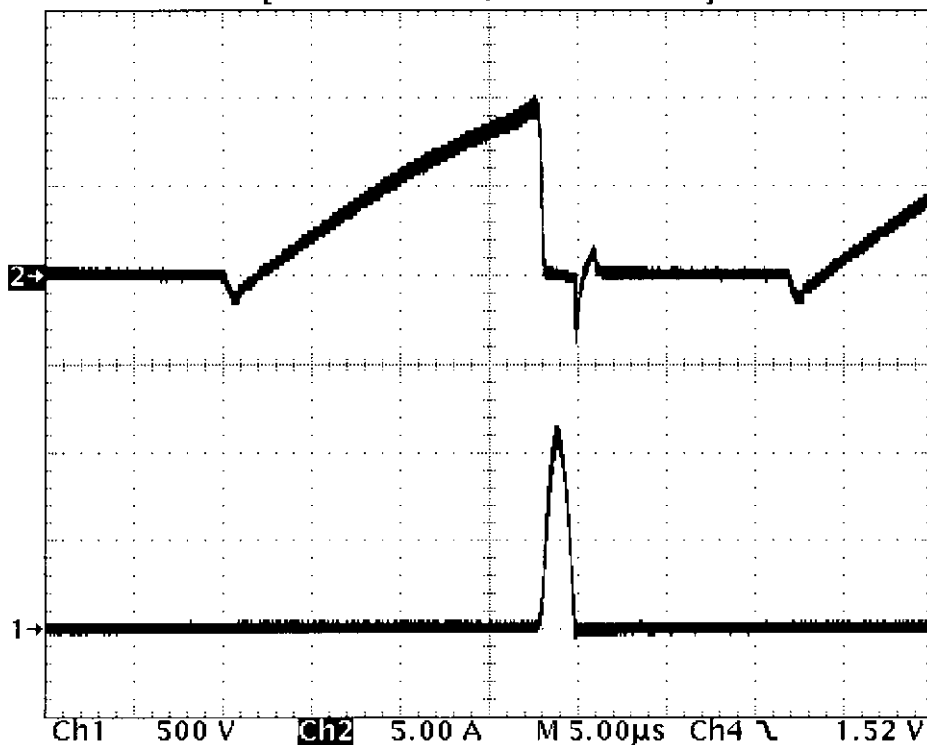


Q502 Ib
(fh=31.5k)

-7Ao-p

Q502 Vbe
(fh=31.5k)

Tek **Stop:** 100MS/s 103689 Acqs DPO Brightness: 20 %



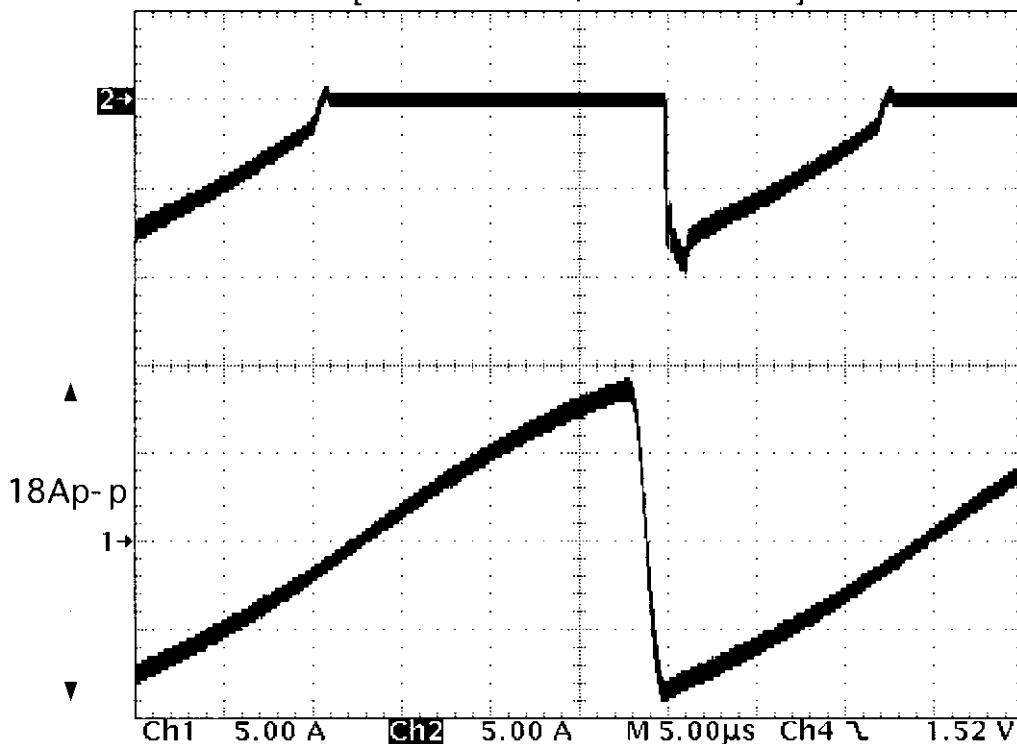
9Ao-p

Q502 I_c
(fh=31.5k)

1150Vp

Q502 V_{ce}
(fh=31.5k)

Tek **Stop:** 100MS/s 205878 Acqs DPO Brightness: 20 %



Damper diode
Current waveform
(fh=31.5k)

-9Ao-p

18Ap-p

I_{dy}
(fh=31.5k)

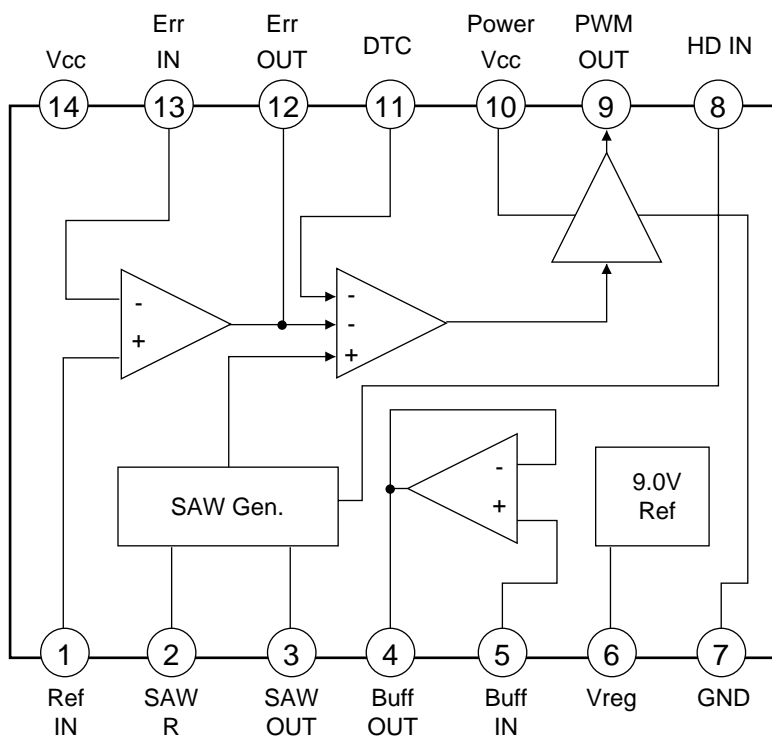


Figure 8. IC5J1 block diagram

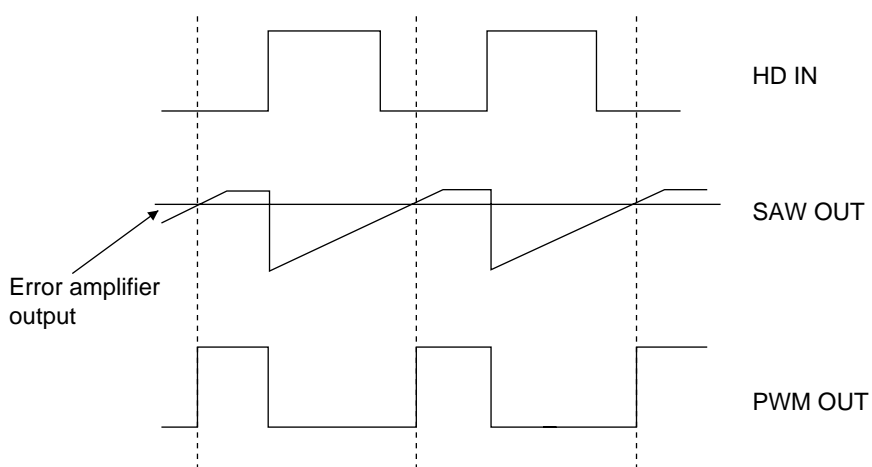


Figure 9. Operation image

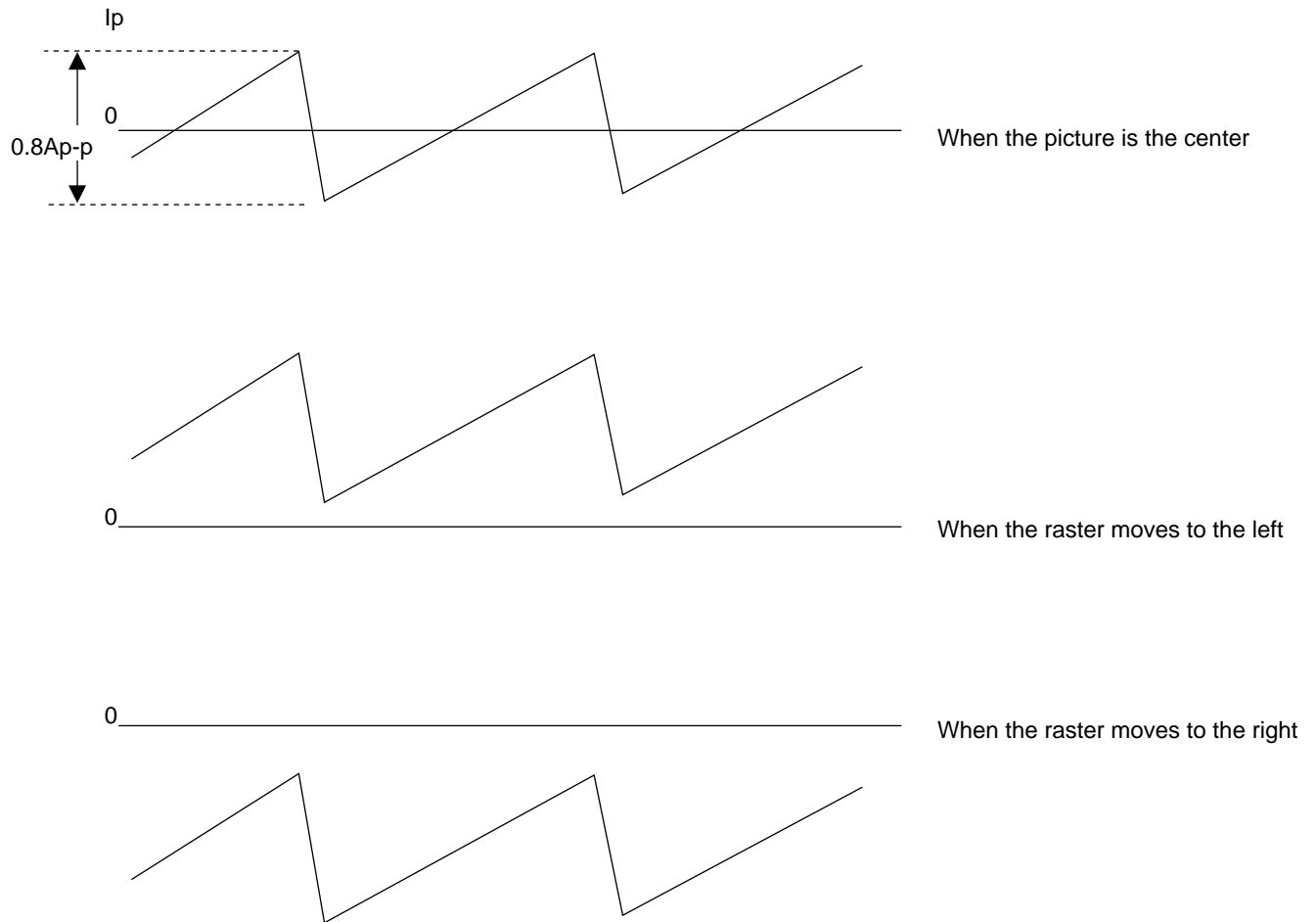


Figure 10 Horizontal position adjustment image

1.2.2 Deflection current compensation circuit

As the picture becomes flatter, the arrival distance of the deflected electronic beam becomes more different between the center and both ends of the picture. Therefore, there is a tendency for the image to be contracted at the center of the picture and expanded at both ends of the picture. Moreover, the left side of the picture is more expanded than the right side of the picture owing to the characteristics of the circuit. CS applies S type compensation to the deflection current with the resonant effect of the deflection yoke and contracts at both ends of the horizontal axis. The linearity coil increases the inductance of the starting section of the deflection current with the supersaturated reactor, and works to contract the left side of the horizontal axis.

As the frequency is lower, the capacity of CS is generally increased and the linearity coil with a larger impedance value is used. In the practical circuit, seven CS capacitors are prepared, and are combined as desired. The linearity coil changes inductance by letting the control current corresponding to the horizontal frequency flow to the control coil.

(1) S type compensation with CS

CS is switched in seven steps by FET. IC501 element with six FETs included and Q510 are used. On IC501, pins 2, 5, 7, 9, 11 and 13 are used as the gate, and pins 3, 6, 8, 10, 12 and 14 are used as the drain. Pins 1 and 15 are used as the ground, and each source are grounded to the earth. The binary value signal of HIGH (5V) or LOW (0V) is input to each gate by IC102. In case of HIGH, FET is turned ON. In case of LOW, FET is turned OFF. The correspondence to the signals from the capacitor and IC102 are as follows.

Table 3

	G	D	Capacitor	Signal
FET1	2	3	C523	CS2
FET2	5	6	C524	CS1
FET3	7	8	C525	CS5
FET4	9	10	C526	CS6
FET5	11	12	C527	CS3
FET6	13	14	C528	CS4
FET7 (Q510)	—	—	C529	CS7

The column of G and D is Pin No.

(2) Compensation with linearity coil

The linearity coil compensates the left expansion of raster by changing the inductance value through the current value flow in order to keep the horizontal linearity to appropriate level. In the actual circuit, L540 stands for the linearity coil.

The newly adopted linearity coil is provided with a control winding capable of controlling the current characteristics of the inductance value. The control voltage (DC) corresponding to each horizontal frequency is supplied from pin 2 of IC101 to pass the control current to the control winding through IC103 and Q540. This controls the current characteristics of the inductance value, and eventually keeps the horizontal linearity to appropriate level. An image of characteristic of linearity coil is as figure 11.

As shown in the Table 4 below, CS is switched on the horizontal frequency bands. 1/0 in the table express the signals from IC101 with 1 for HIGH and 0 for LOW. Here, the column of the frequency expresses the lower limit value.

User Timing

Table 4

Fh (kHz)	CS7	CS6	CS5	CS4	CS3	CS2	CS1	com	total
	0.024	0.056	0.15	0.24	0.47	0.82	1.3	0.173	
31	1	1	1	1	1	1	1	0.173	3.233
34	0	0	0	1	0	1	1	0.173	2.533
36.5	0	0	1	0	0	1	1	0.173	2.443
39	0	0	1	1	1	1	0	0.173	1.853
45	0	1	0	0	1	1	0	0.173	1.519
47.5	0	1	0	0	1	1	0	0.173	1.519
49	1	1	1	1	1	0	0	0.173	1.113
52	1	1	1	1	1	0	0	0.173	1.113
55	0	0	1	1	1	0	0	0.173	1.033
59	1	0	0	1	1	0	0	0.173	0.907
61	0	0	0	1	1	0	0	0.173	0.883
63	0	0	0	1	1	0	0	0.173	0.883
66	1	1	1	1	0	0	0	0.173	0.643
70	1	1	1	1	0	0	0	0.173	0.643
73	0	1	1	1	0	0	0	0.173	0.619
76	0	0	1	1	0	0	0	0.173	0.563
78.5	1	1	0	1	0	0	0	0.173	0.493
81.5	0	1	0	1	0	0	0	0.173	0.469
83	0	1	0	1	0	0	0	0.173	0.469
86.5	0	1	1	0	0	0	0	0.173	0.379
89	0	1	1	0	0	0	0	0.173	0.379
92	0	0	1	0	0	0	0	0.173	0.323
94	0	0	1	0	0	0	0	0.173	0.323
97	0	0	1	0	0	0	0	0.173	0.323
104	1	1	0	0	0	0	0	0.173	0.253
108	1	1	0	0	0	0	0	0.173	0.253
111	0	1	0	0	0	0	0	0.173	0.229
114	0	1	0	0	0	0	0	0.173	0.229
116	1	0	0	0	0	0	0	0.173	0.197
125	0	0	0	0	0	0	0	0.173	0.173

Preset Timing

timing	CS7	CS6	CS5	CS4	CS3	CS2	CS1	com cs	total Cap.
	0.024	0.056	0.15	0.24	0.47	0.82	1.3		
31k/60	1	1	1	1	1	1	1	0.173	3.233
46k/75	0	1	0	0	1	1	0	0.173	1.519
60k/75	1	0	0	1	1	0	0	0.173	0.907
68k/85	0	1	1	1	0	0	0	0.173	0.619
80k/75	0	0	1	1	0	0	0	0.173	0.563
91k/85	1	1	1	0	0	0	0	0.173	0.403
93k/75	0	0	1	0	0	0	0	0.173	0.323
106k/85	1	1	0	0	0	0	0	0.173	0.253
112k/75	0	1	0	0	0	0	0	0.173	0.229
120k/85	1	0	0	0	0	0	0	0.173	0.197

1: ON 0: OFF

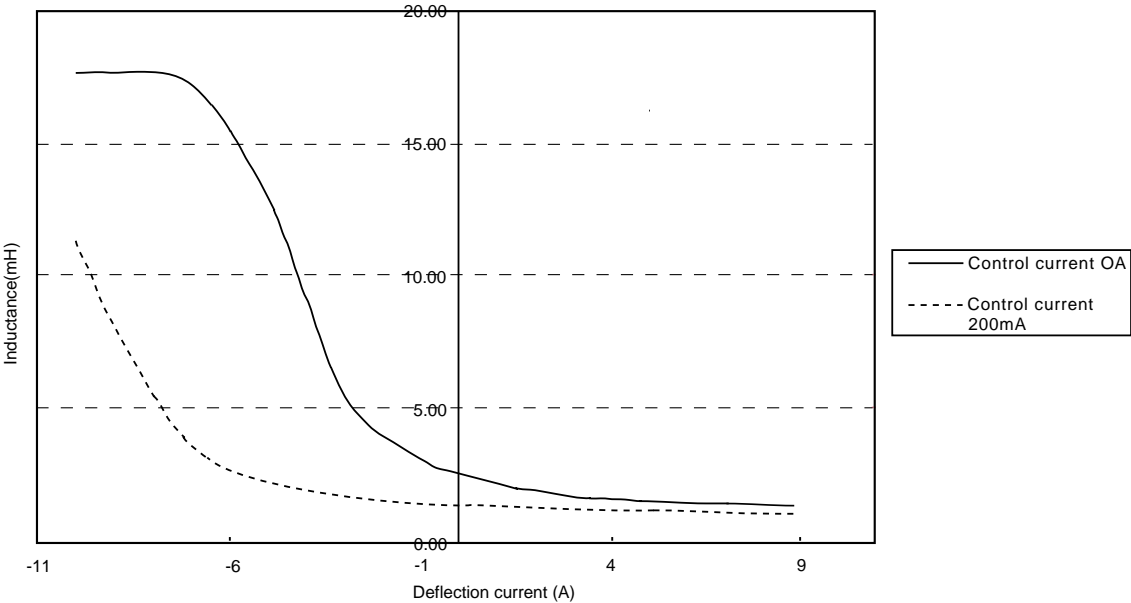
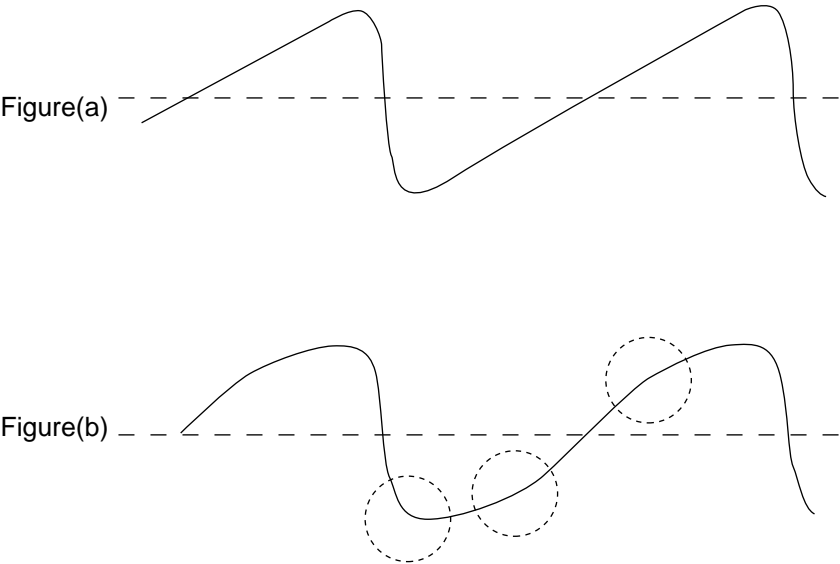


Figure 11 Characteristic of variable lineality

The waveform of the deflection current is compensated from Fig. (a) to Fig. (b) through the above. The starting section of the current is smoothened, and the linear section becomes the S type.



1.3 Vertical output block

The vertical deflection circuit controls the vertical width and vertical position with IC601 on the DEFL_SUB substract, and IC603 controls the linearity. Moreover, the signal output from IC603 is input to the vertical deflection output IC401.

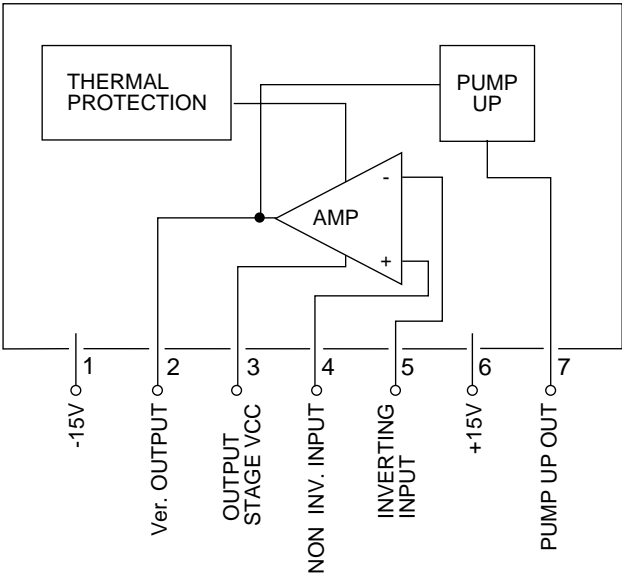


Figure 12 IC401(LA7841L) Pin connection & Function Block diagram

1.4 High voltage block

The high voltage circuit is composed of the high-voltage regulator IC701, MOS-FET Q701 flyback transformer (FBT) T701, operation amplifier IC702 and their peripheral circuits.

1.4.1 High voltage control circuit

The IC701 is an IC for high voltage control, with the block diagram given in Fig.13. The OFF trigger PWM control system is adopted to carry out high voltage control. The built-in VCO circuit gets synchronized when the horizontal synchronous signal (hereafter SYNC signal) is input from Pin 3 of IC701 (horizontal synchronous input terminal). Thus, the MOS-FET Q701 is controlled to turn OFF with the timing of the SYNC signal changing over to HI, and is called OFF trigger system.

Further, the DC voltage, output after the feedback signal (IC701 Pin 11) from FBT T701 is compared with the high-voltage set voltage (IC701 Pin 12) from IC101 in the internal error amplifier, is compared with the saw-tooth-waveform of VCO to control the pulse output DUTY so as to keep the high voltage constant (PWM control).

The timing chart for OFF trigger PWM control system is given in Fig.14. Set the high voltage by selecting [HVADJ] in OSD and manipulating +/- button (Standard value: 27.0kV).

1.4.2 Protective function circuit

(1) Start and stop of high-voltage regulator IC701

The IC701 starts operation when Vcc voltage (power voltage applied to Pin 2 and Pin 10) attains the level of 8.4 V_{typ}, and the operation stops when the Vcc voltage is less than 7.4 V_{typ}.

(2) IC701 overcurrent protection (OCP) function

It detects the peak value of the drain current in MOS-FET Q701 per pulse and stops DRIVE when the voltage in Pin 6 of IC701 detecting the end-to-end voltage of the source resistors (R706 and R707), exceeds 1.0 V_{typ} until the next SYNC signal is input.

(3) IC701 overload protection (OLP) function

This function brings the system to the latch stop when OCP gets continuously activated due to continuous overload.

It forms time constant using C716. With OCP activated and C716 charged and the voltage in Pin 8 of IC701 exceeding 2.5 V_{typ}, IC701 gets set to Latch mode, bringing the control operation to stop. This status does not get released (reset) until the Vcc voltage (power voltage applied to Pin 2 and Pin 10) in IC701 is less than 7.4 V_{typ}.

(4) Over-voltage protection function for anode voltage (X-ray protector)

A voltage proportional to the high voltage is generated in Pin 6 of T701 due to the winding ratio between secondary and tertiary winding inside FBT T701. This voltage is then rectified by D707 and C708 and is further divided by R708 and R709 before being input in Pin 17 of microcomputer IC101 for comparison with the X-Pro set value. In case the voltage exceeds the set value, the output in Pin 33 of microcomputer IC101 gets fixed to LOW (P-OFF mode). With the mode set to P-OFF, the application of voltage Vcc to IC701 stops, causing the IC701 operation to stop. The status continues until the power SW is turned OFF. The overvoltage protection function is set to operate when the high voltage level reaches 30kV (with the beam current is approx. 1mA).

(5) Overcurrent protection function for beam current (beam protector)

The beam current is supplied from +12V power source through R722. Since the end-to-end voltage of R722 varies according to the beam current, the voltage drop due to R722 becomes large if the beam current increases. The voltage in Pin 9 of FBT T701 (the voltage obtained by subtracting the voltage drop due to beam current from the +12V power voltage) undergoes resistance division by R723 and R724, and is then input into Pin 6 of operation amplifier IC702 for comparison with Pin 5 of IC702 (reference voltage). The voltage is then output (Pin 7 of IC702) and is input into Pin 16 of microcomputer IC101. The voltage in Pin 7 of IC702 (output terminal) is output linearly due to the fluctuation in beam current. However, if the terminal voltage in Pin 16 of IC101 exceeds Beam-Pro setting value (ABL data +70 : Max. 254), the output of Pin 33 of IC101 gets fixed to LOW (P-OFF mode). With the mode set to P-OFF, the application of Vcc voltage to IC701 stops, causing the IC701 operation to stop. This status continues until the power switch is turned OFF. The overcurrent protection function is set to operate when the beam current reaches the level of approximately 1300μA.

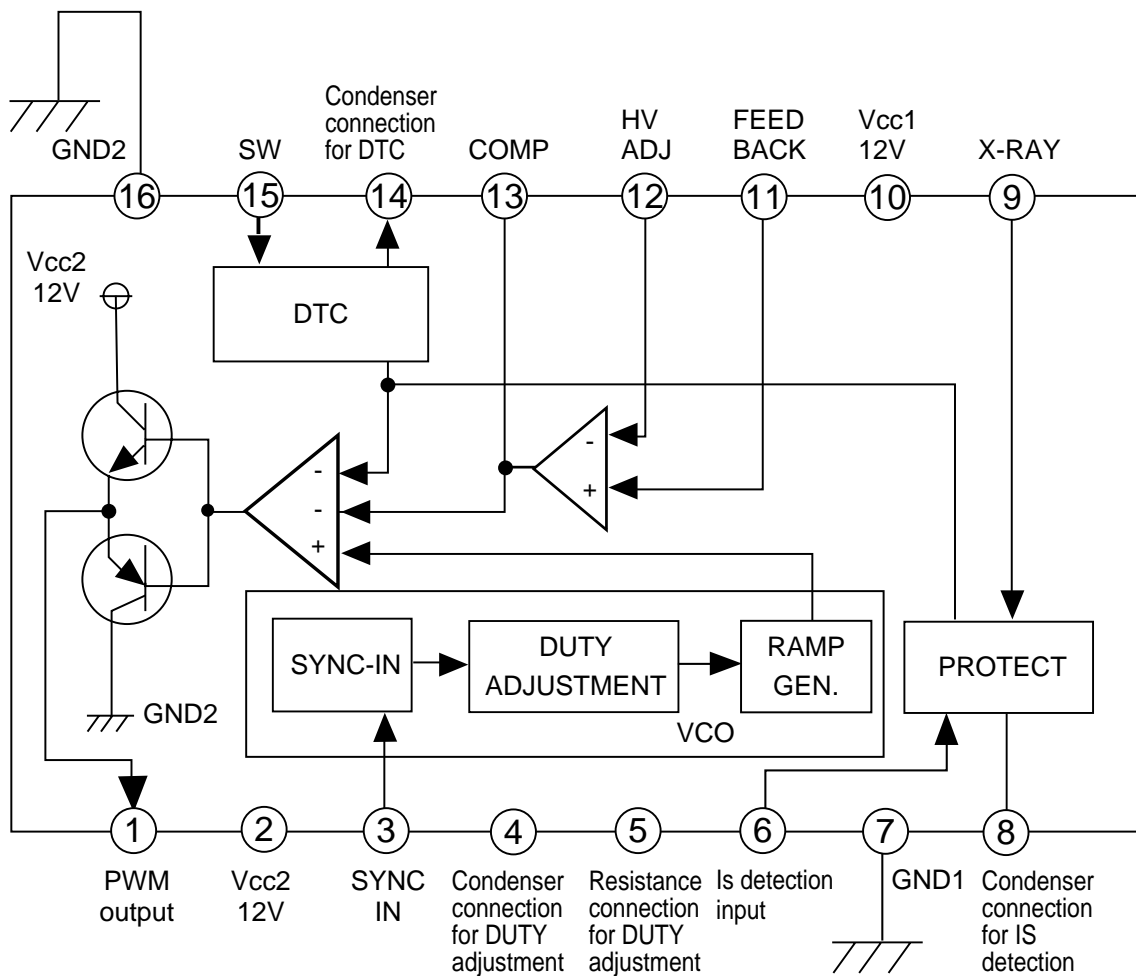


Figure 13. High voltage regulator IC701 block diagram

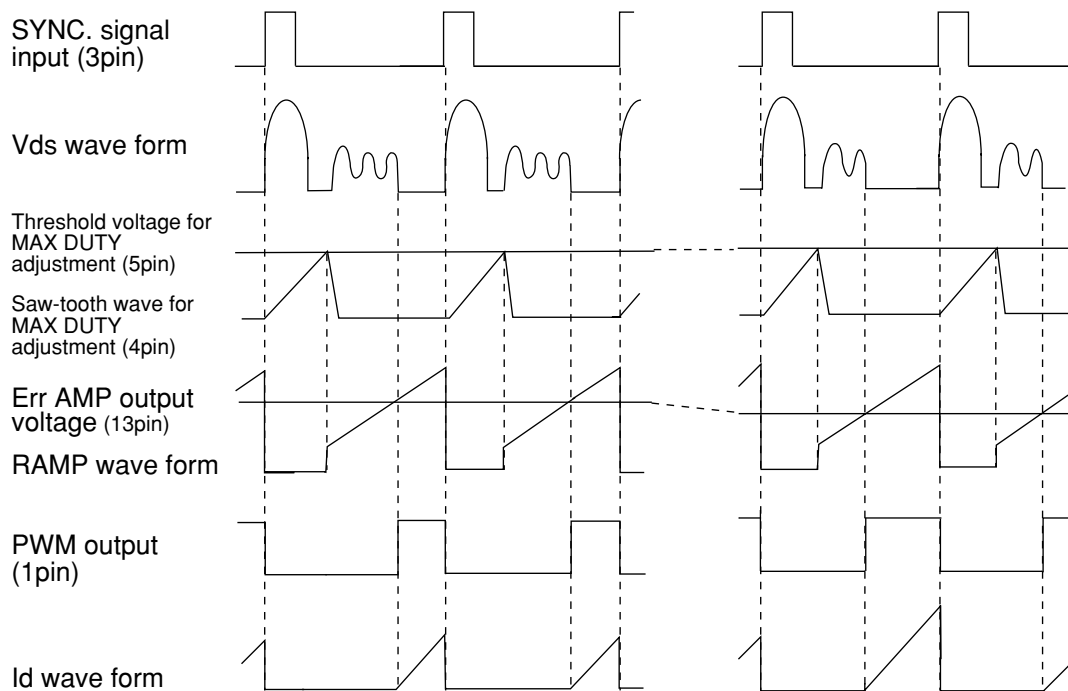


Figure 14. OFF trigger PWM control system timing chart

1.4.3 DBF (Dynamic Beam Focus) circuit

Since the display is flattened, the focus becomes unequal between the center and circumference of the picture. To compensate for it, it is necessary to superimpose the parabola voltage of 370Vp-p in the horizontal cycle with the static focus (with the horizontal width is 396mm) and the parabola voltage of 145Vp-p in the vertical cycle. The slight voltage that is generated from the parabola voltage generating circuit is amplified and reversed to generate the high voltage in order to keep the focus equal. This circuit is called DBF circuit.

As shown in Fig. (16), the circuit is composed of the parabola voltage generating circuit IC601, amplifier section IC6A1 in the front step, Q7A1 to Q7B5 of amplifier section in the rear step, T7A1, and so on.

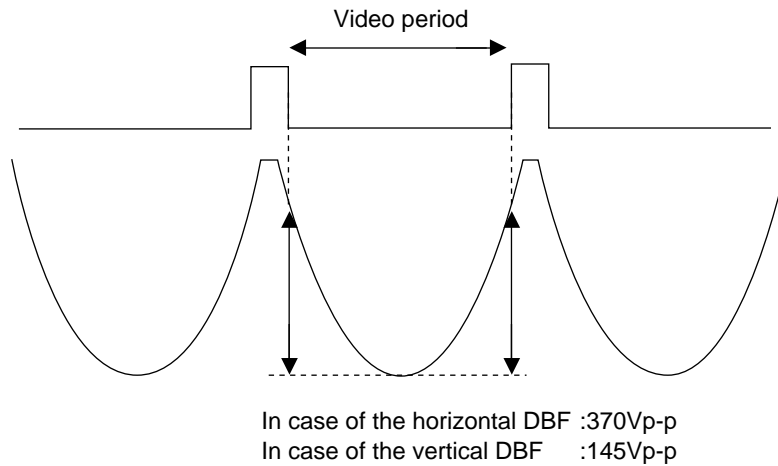


Figure 15

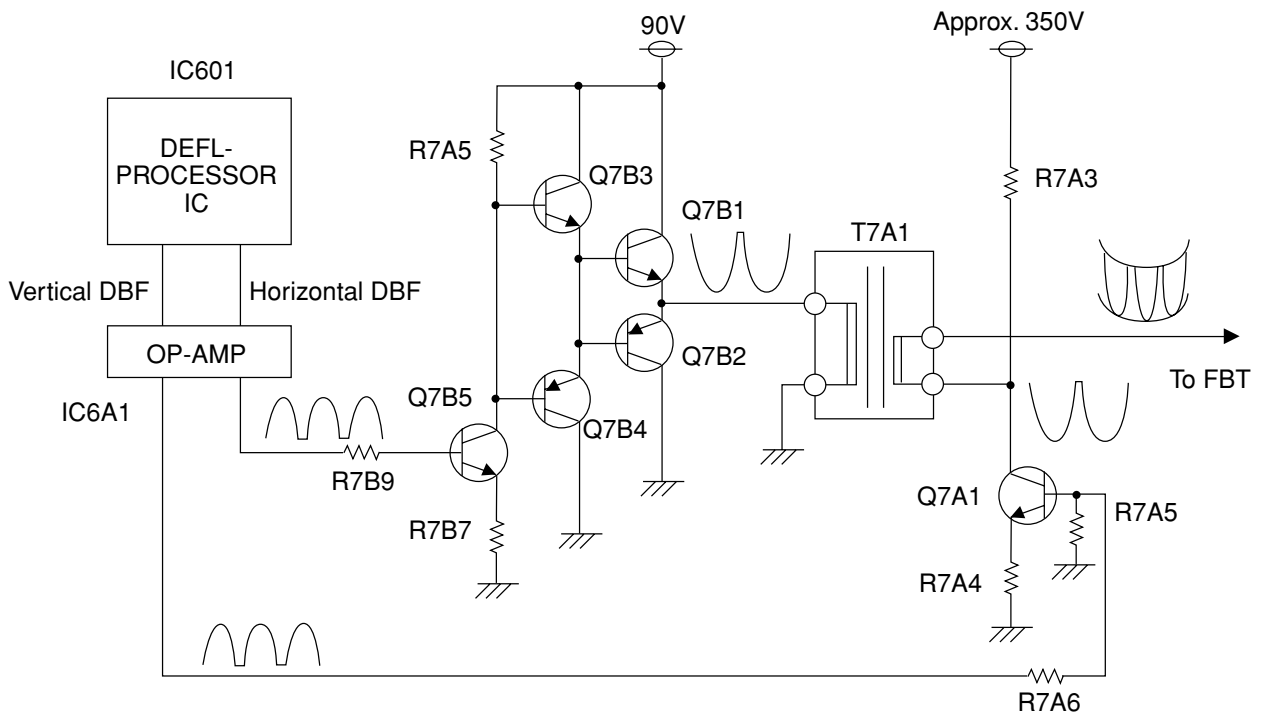


Figure 16

After the horizontal and vertical DBF voltage are separately generated, they are amplified and are finally composed.

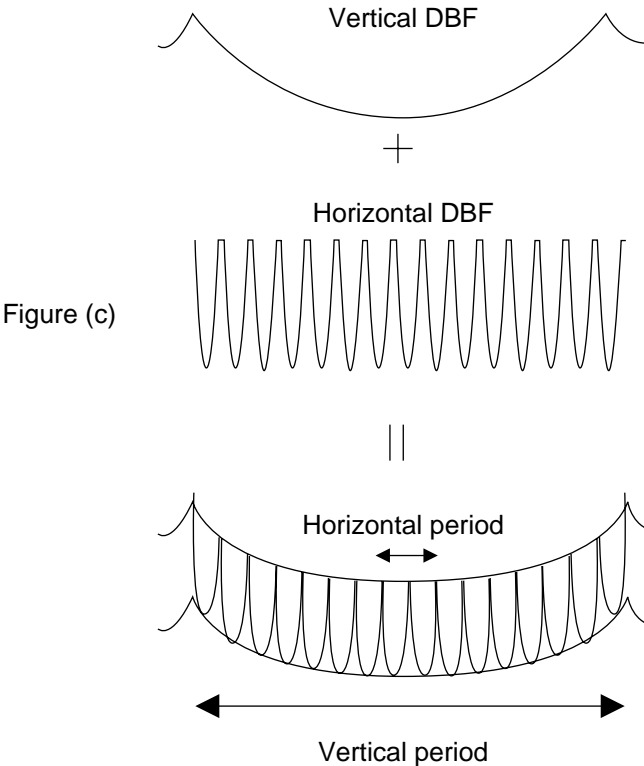
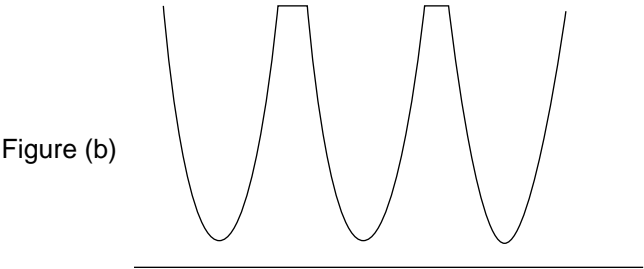
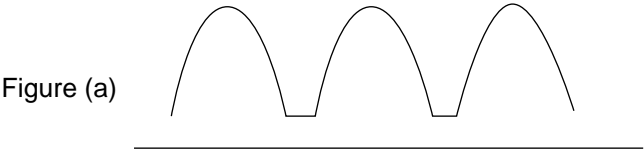
<Horizontal section>

The voltage (approx. 0.5Vp-p) of the parabola waveform shown in Fig. (a) is output from the deflection processor IC (IC601), and is amplified approx. 10 times by OP-AMP (IC6A2). Thereafter, it is amplified to 50 to 60Vp-p by the transistor (Q7B1 and Q7B2). The amplification ratio is determined by the ratio between the resistors R7B6 and R7B7, being approx. 10 times. Moreover, the waveform is reversed as shown in Fig. (b) at this time. Then, it is amplified to approx. 500Vp-p by DBF transformer (T7A1). The coil ratio between the primary and secondary coils of the DBF transformer is 1: 10, being the amplification ratio of approx. 10 times.

<Vertical section>

The voltage (approx. 1.0Vp-p) of the parabola waveform shown in Fig. (a) is output from the deflection processor IC (IC601), and is amplified approx. 4 times by OP-AMP (IC6A2). Thereafter, it is amplified to approx. 160Vp-p by the transistor (Q7A1). The amplification ratio this time is determined by the ratio between R7A3 and R7A4, being approx. 40 times.

The horizontal and vertical DBF voltages amplified and reversed are composed by applying vertically synchronous modulation to the output on the secondary side as shown in Fig. (c). The composed voltage is input to Pin 12 of the flyback transformer (T701).



1.5 CRT compensation block

1.5.1 Rotation circuit

The rotation circuit is a circuit to compensate the picture inclination caused by the earth magnetism by letting DC current flow to the rotation coil wound on the front side of DY for adjustment. It is controlled to 0 to 5V with the reference of 2.5V by IC103 pin 3 (PWM_DAC), and DC current of +/-90mA (max) is made to flow to the rotation coil by IC804 pin 2.

This correction circuit has two functions; (1) User adjustment (OSD display) and (2) Southern/Northern horizontal magnetic field rotation cancellation, as follows.

(1) User adjustment (OSD display)

User provides DC current to the rotation coil according to the value displayed on OSD.

(2) Southern/Northern horizontal magnetic field rotation cancellation

Southern/Northern horizontal magnetic field rotation cancellation is to automatically adjust the variation of raster rotation by earth magnetism.

Detection voltage and direction of the southern/northern horizontal magnetic field (pin 2 of IC214) is detected by IC214 (Earth magnetism sensor unit), and pin 18 of IC101

(CPU_ADC) reads the detected voltage and provides DC current to the rotation coil according to the prescribed control program.

1.5.2 Corner purity circuit

The corner purity circuit is a circuit to compensate for the color shade and color deviation of the picture corner. On the rear side of CRT, it is adjusted by DC current flowing to the corner purity coils installed in the four corners on the display surface.

The compensation circuit is composed of the following four functions of (1) User adjustment (OSD display), (2) Aging variation compensation, (3) High/low temperature drift compensation and (4) Southern / Northern horizontal magnetic field landing cancellation.

(1) User adjustment (OSD display)

The user causes DC current of +/-60mA (max.) to flow to the purity coil of each corner according to the value displayed on OSD.

(2) Aging variation compensation

As the electronic beam collides with the aperture grille, it is thermally expanded and contracted. The thermal expansion/contraction is varied according to the elapse of the power ON/OFF time of the monitor. The color shade and deviation of the picture corner thus generated are automatically adjusted.

The voltage of the beam current supply pin (T701 pin 9) is detected with R723/R724, and the voltage that detects the time elapse of the power ON/OFF of the monitor is read from the CR charge (integration) circuit composed of C723 and R736 and CR discharge (integration) circuit, composed of C723 and R737 through IC702 (buffer amplifier) by IC101 pin 15 (CPU_ADC), and the DC current of +/-17mA(max) flows to the purity coil on each corner according to the specified control program.

(3) High/low temperature drift compensation

The front panel (glass) is thermally expanded and contracted as the temperature varies in the installation environments of the monitor. The color shade and deviation of the picture corner are automatically adjusted. The voltage that detects the temperature variation of the installation environments of the monitor is read from the environment temperature detection circuit composed of TH101 (thermistor) arranged near the front panel (glass) by IC101 pin 14 (CPU_ADC), and DC current of +/-13mA (max) is made to flow to the purity coil on each corner according to the specified control program.

(4) North-south horizontal field landing cancel

The north-south horizontal field landing cancel carries out automatic adjustment of color shading and color shift occurring appeared in the opposite direction at the top and bottom end of the monitor display surface in the horizontal direction.

The detecting voltage and direction of the north-south horizontal field (IC214 pin 2) are detected by IC214 (geomagnetic sensor unit), the detecting voltage is read by IC101 pin 18 (CPU_ADC), and the direct current of $\pm 20\text{mA}$ (max) flows in each corner purity coil according to the specified control program. (Four-corner interlock control)

- The left upper corner on the display surface is controlled with 0 to 5V of 2.5V reference by IC101 pin 6 (PWM-DAC), and the DC current of the above value is made to flow to the purity coil on the left upper corner by IC803 pin 2.
- The right upper corner on the display surface is controlled with 0 to 5V of 2.5V reference by IC101 pin 7 (PWM-DAC), and the DC current of the above value is made to flow to the purity coil on the right upper corner by IC803 pin 8.
- The left lower corner on the display surface is controlled with 0 to 5V of 2.5V reference by IC101 pin 8 (PWM-DAC), and the DC current of the above value is made to flow to the purity coil on the left lower corner by IC801 pin 2.
- The right lower corner on the display surface is controlled with 0 to 5V of 2.5V reference by IC101 pin 9 (PWM-DAC), and the DC current of the above value is made to flow to the purity coil on the right lower corner by IC801 pin 8.

1.5.3 Earth magnetism cancel circuit

The earth magnetism cancel circuit has a south-north horizontal magnetic field canceling function and a vertical magnetic field canceling function.

IC214 (earth magnetism sensor unit) detects the voltage and direction of the south-north horizontal magnetic field (IC214 pin 2) and the vertical magnetic field (IC214 pin1), and IC101 pins 18 and 19 (CPU_ADC) reads the detected voltage to automatically control the following canceling function according to the specified control program.

Here, the output voltage of IC214 (earth magnetism sensor unit) operates as follows.

- South-north horizontal magnetic field (IC214 pin 2): $0.8\text{V}(-0.04\text{mT})$ to $2.5\text{V}(+/-0.00\text{mT})$ to $4.2\text{V}(+0.04\text{mT})$
- Vertical magnetic field (IC214 pin 1) : $3.3\text{V}(-0.04\text{mT})$ to $2.5\text{V}(+/-0.00\text{mT})$ to $0.5\text{V}(+0.10\text{mT})$

<South-north horizontal magnetic field canceling function>

(a) Horizontal magnetic field landing cancel

The horizontal magnetic field landing cancel circuit is a circuit to compensate for the color shade and deviation that appear in the horizontal direction that becomes the opposite direction at the upper and lower ends on the monitor display surface, and the automatic adjustment is done by DC current flowing to the corner purity coil that is wound around the display surface. (synchronized control for four corners)
(Refer to 1.5.2 (4) for detail.)

(b) Horizontal magnetic field convergence cancel

The horizontal magnetic field convergence cancel circuit is the circuit to compensate for the misconvergence that results after the vertical convergence of RED and BLUE in the whole display area of the monitor deteriorates, and it is automatically adjusted by DC current flowing to the 4V convergence compensation coil mounted on DY. It is controlled with the DC component (V-CONVERGENCE) by IC601 pin 60 (4V_SC), and DC current of $\pm 30\text{mA}$ (max) is flown to the 4V convergence compensation coil by IC8A1 pin 6 (Power Opamp).

<Vertical magnetic field canceling function>

(a) Landing compensation

VCANCEL_S (Schematic Diagram) and PWB-VCANCEL (PWB) are added so that the CRT specified for Northern Hemisphere ITC can be adjusted to the spec for Southern Hemisphere ITC.

Some circuits are also added to DEFL-SUB (Schematic Diagram) and PWB-DEFLSUB (PWB).

In PWB-VCANCEL a vertical sync. parabola waveform output from pin 59 of IC601 (1 bit DAC) is supplied from pin 6 of J804 via pin 6 of J8P0 and 300mA_{p-p} parabola waveform (vertical sync.) current flows to the speed modulation coil from pin 1 of J8P1 via Q8P0 and Q8P1.

In PWB-DEFLSUB a vertical sync. parabola waveform output from pin 59 of IC601 (1 bit DAC) is reversed and amplified via Q600 and it is associated to the horizontal phase deflection compensation waveform output from pin 57 of IC601 to compensate side pin balance.

(b) Vertical magnetic field landing cancel

The vertical magnetic field landing cancel circuit is the one to compensate the color shade and deviation that reaches its maximum at the center in the horizontal axis direction and its minimum at the upper and lower ends on the monitor surface.

The automatic adjustment is done by controlling DC level of the above 300mA_{p-p} parabola waveform flowing to the speed modulation coil installed in the neck part of CRT.

It is controlled by pin 4 of IC101 (PWM-DAC "VCANCEL"), and controls the speed modulation coil with DC level of $\pm 50\text{mA}$ by Q8P0 and Q8P1.

(c) Vertical magnetic field convergence cancel

The vertical magnetic field convergence cancel circuit is the circuit to compensate for the misconvergence that results after the vertical convergence of RED and BLUE reversed at the upper and lower ends on the whole display area of the monitor deteriorates, and it is automatically adjusted by the saw-toothed waveform (vertical-frequency) current flowing to the 4V convergence compensation coil mounted on DY. It is controlled with the AC component (YVJT & YVJB, vertical frequency saw-toothed waveform) by pin 60 of IC601 (4V_SC), and saw-toothed waveform (vertical frequency) current of $\pm 45\text{mA}$ (peak) is made to flow to the 4V convergence compensation coil by pin 6 of IC8A1 (PowerOpamp).

1.5.4 Digital dynamic convergence clear (DDCC) circuit

In the digital dynamic convergence clear (hereafter called DDCC) circuit, the convergence compensating current waveform is produced and amplified, and the convergence is compensated by the compensation current flowing to the sub yoke that is installed as the rear unit of the deflection yoke.

Though the principle of the convergence compensation with the sub yoke is same as the CP ring, the CP ring is used for the static variation with the parallel movement in the whole picture in the uniform magnetic field with the permanent magnet but the sub yoke is used for dynamic variation that compensates a desired position on the picture by controlling the current waveform that flows to the coil of the electric magnet.

(See Fig. 18)

(1) Production of compensation current waveform

There are 30 kinds of compensation elements, and they are programmed in IC601(CP267P151=uPD61882BGC) one by one by using the functions. The amplitude of the current is controlled by inputting the compensation coefficient into the function.

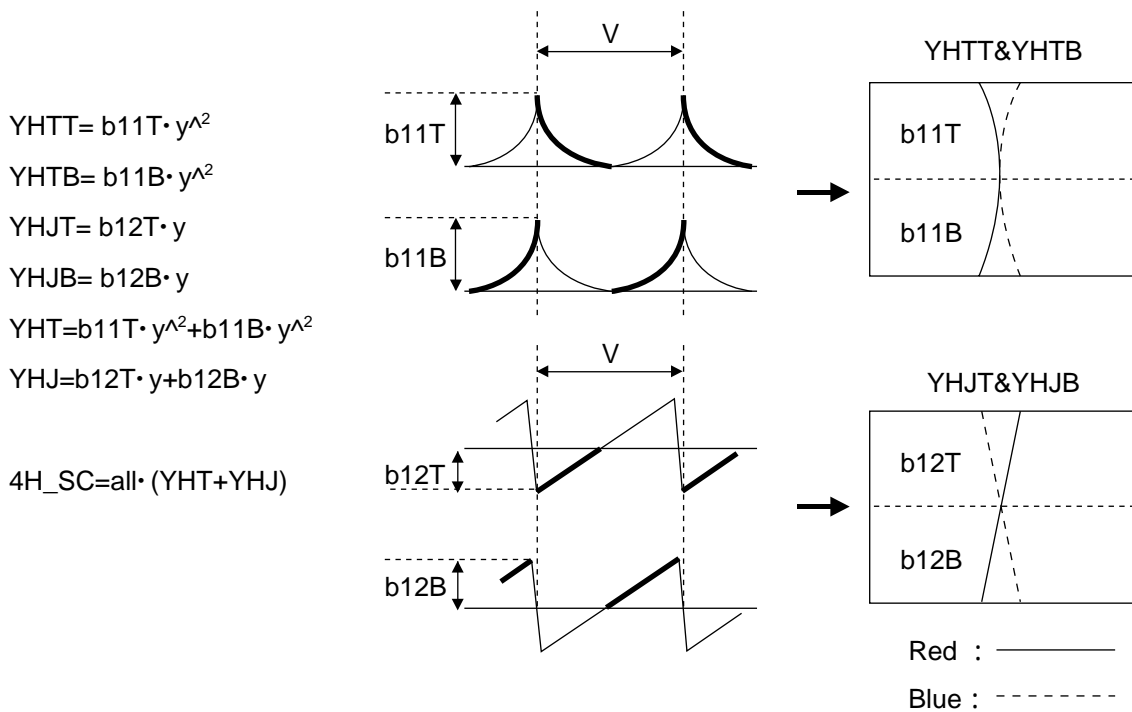


Figure 17 DDCC compensation image

Examples of the functions and current waveform/compensation operation of YH(YHTT, YHTB, YHJT, YHJB) are shown as follows.

In the above formulas, b_{11T} , b_{11B} , b_{12T} and b_{12B} express the compensation coefficients, and y and y^2 express the primary and secondary functions of the vertical frequencies. The other parts except the compensation coefficients are programmed, and desired amplitudes (= compensation amount) are gained by varying the coefficients.

YHTT and YHTB compensate the upper and lower parts of the picture of the characteristic components of their DYs to compensate the upper and lower parts of the picture of the axis deviation component. The component gained by adding YHT and YHJ is multiplied by the offset compensation coefficient a_{11} . The resultant component is regarded as $4H_SC$, and is output from IC601 (CP267P151=uPD61882BGC) pin 61.

(2) Waveform, and operation on the picture

The case in which the currents flow through 4H coils of the sub yoke is explained. Regarding YHT (secondary function in the vertical frequency), in case of Fig 17 as an example, the current is large in the same direction at the start (upper end of the picture) and the end (lower end of the picture) of the vertical frequency, and is zeroed on the X axis of the picture. Therefore, the magnetic field that is proportional to it is generated, and RED and BLUE vary in the same direction only at the upper and lower ends of the picture. As aforementioned, YHT can be independently controlled at the upper part ($b11T.y^2$) and lower part ($b11B.y^2$).

Moreover, regarding YHJ (Primary function in the vertical frequency), if the flowing direction of the current is opposite at the start (upper end of the picture) and the end (lower end of the picture) of the vertical frequency as an example, RED and BLUE vary in the opposite direction only at the upper and lower ends of the picture. Compensation in the vertical direction can be done by making the current flow to the 4V coil.

Fig.19(a) and (b) shows the image of each adjustment item of the DDCC adjustment.

(3) Adjustment method

Before the adjustment with the compensation circuit, it is necessary that they are properly adjusted at the center (H-STATIC and V-STATIC), on the X axis (XH slider, B-Bow 4P, XV differential coil) and on the Y axis (YH volume, YV volume).

Though DC current is superimposed on the sub yoke, H-STATIC and V-STATIC are pushed to the greatest possible extent by the adjustment with CP ring in order to reduce the stress of the driver IC8A1 (STK391-110).

Moreover, since 4H and 4V coils alone are installed on the chassis, it is first necessary that the convergence of RED, BLUE and GREEN (6H, 6V) satisfy the specifications for the performance of ITC(CRT&DY).

As the adjustment procedure, the adjustment values of 30 elements are not respectively zeroed but they are adjusted to nearest to zero with a total balance in good order.

In other words, the balance (compromise) adjustment with each adjustment item is applied.

The correspondence of the names of DDCC adjustment mode to the coefficients of all 30 elements is shown below.

< Factory mode >

4H Coil	b11T	YHTT	y^2	b11B	YHTB	y^2	b12T	YHJT	y	b12B	YHJB	y
	b21L	XHL	x^2	b21R	XHR	x^2						
	b31TL	S3HTL	$x^2 \cdot (-y^3+y^4+y^5+y^6)$	b31TR	S3HTR	$x^2 \cdot (-y^3+y^4+y^5+y^6)$	b31BL	S3HBL	$x^2 \cdot (-y^3+y^4-y^5+y^6)$	b31BR	S3HBR	$x^2 \cdot (-y^3+y^4-y^5+y^6)$
	b41TL	PQHTL	$x^2 \cdot y^4$	b41TR	PQHTR	$x^2 \cdot y^4$	b41BL	PQHBL	$x^2 \cdot y^4$	b41BR	PQHBR	$x^2 \cdot y^4$
4V Coil	c11T	YVTT	y^2	c11B	YVTB	y^2	c12T	YVJT	y	c12B	YVJB	y
	c21L	XVL	x^2	c21R	XVR	x^2						
	c31TL	S3VTL	$x^2 \cdot (-y^3+y^4+y^5+y^6)$	c31TR	S3VTR	$x^2 \cdot (-y^3+y^4+y^5+y^6)$	c31BL	S3VBL	$x^2 \cdot (-y^3+y^4-y^5+y^6)$	c31BR	S3VBR	$x^2 \cdot (-y^3+y^4-y^5+y^6)$
	c41TL	PQVTL	$x^2 \cdot y^4$	c41TR	PQVTR	$x^2 \cdot y^4$	c41BL	PQVBL	$x^2 \cdot y^4$	c41BR	PQVBR	$x^2 \cdot y^4$

< User & Factory mode >

4H Coil	a11	H-CONVERGENCE	DC
4V Coil	a12	V-CONVERGENCE	DC

Table 5

(4) Block diagram

Fig. 20 shows the block diagram of the DDCC circuit.

The components 4H_DC(pin 6), 4H_SC(pin 61), 4V_DC(pin 8) and 4V_SC(pin 60) supplied from IC601(CP267P151=uPD61882BGC) to 4H-Coil and 4V-Coil are output, the dynamic component (4H_DC, 4V_DC) is amplified with IC6A1(TL084), and the static component (4H_SC, 4V_SC) is amplified with IC6A2(KIA4558).

DCC(pin 7) output from IC601 (CP267P151=uPD61882BGC) and DEFL_+3.3V(pin 3) output from IC602 (TA48M033F) are respectively the reference voltage of Op-Amp(IC6A1:TL084) that amplifies the above dynamic component (4H_DC, 4V_DC) and the reference voltage of Op-Amp(IC6A2:KIA4558) that amplifies the static component (4H_SC, 4V_SC).

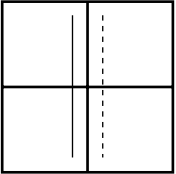
On each of 4H and 4V, the waveform added with the dynamic component and static component is input to IC8A1 pin 3 and pin 4 (STK391-110) allow the specified current to flow to each convergence compensation coil.

<p>Static change by the eternal magnetic field (Parallel shifting totally)</p>	<div data-bbox="571 90 879 399"></div> <div data-bbox="971 112 1257 362"></div>
	<div data-bbox="571 474 879 784"></div> <div data-bbox="971 508 1257 757"></div>
<p>Dynamic change by electromagnet (Compensate at the optional position on the picture.)</p>	<div data-bbox="454 1052 544 1078"><p>4H coils</p></div> <div data-bbox="571 906 879 1215"></div> <div data-bbox="971 934 1257 1183"></div> <div data-bbox="1023 1215 1209 1241"><p>YHT compensate</p></div> <div data-bbox="454 1455 544 1482"><p>4V coils</p></div> <div data-bbox="571 1318 879 1628"></div> <div data-bbox="971 1348 1257 1590"></div> <div data-bbox="1023 1622 1209 1649"><p>YVT compensate</p></div>

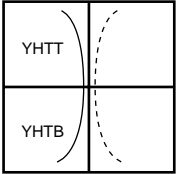
Figure 18 The principle of DDCC compensation

RED —————
BLUE - - - - -

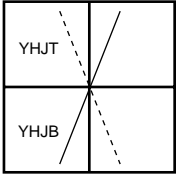
H-CONVERGENCE



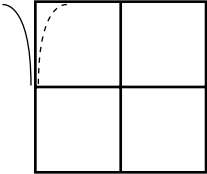
YHTT&YHTB



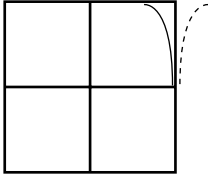
YHJT&YHJB



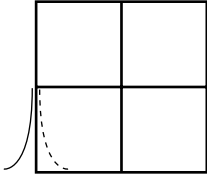
PQHTL



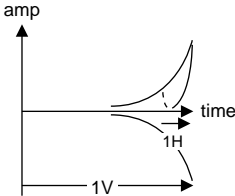
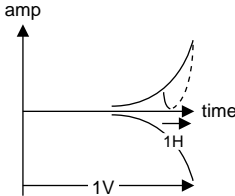
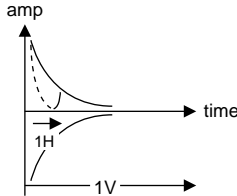
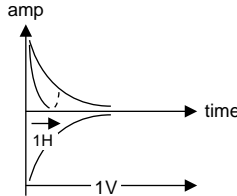
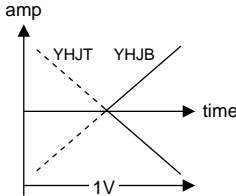
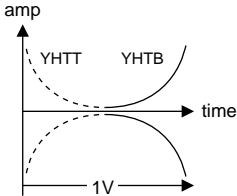
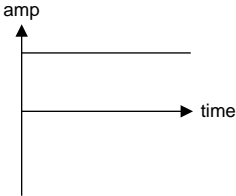
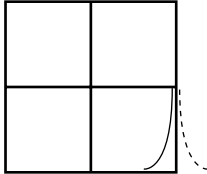
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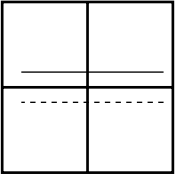
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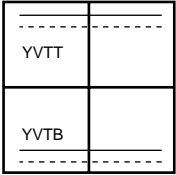
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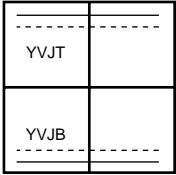
V-CONVERGENCE



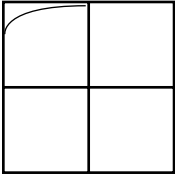
YVTT&YVTB



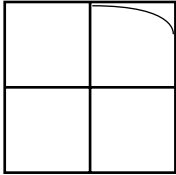
YVJT&YVJB



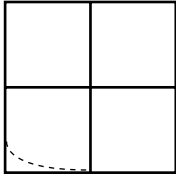
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PQVTR



PQVBL



PQVBR

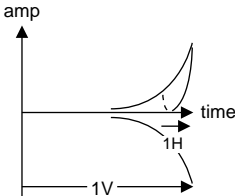
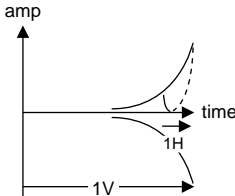
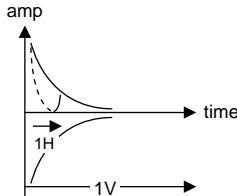
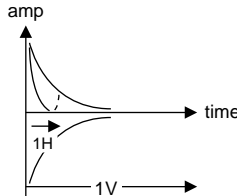
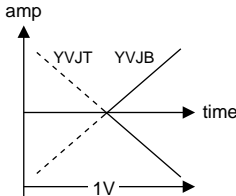
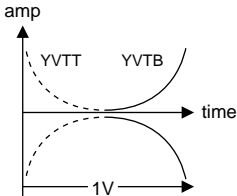
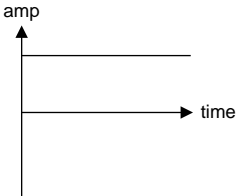
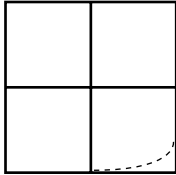


Figure 19 (a) DDCC adjustment item

RED —————
 BLUE - - - - -

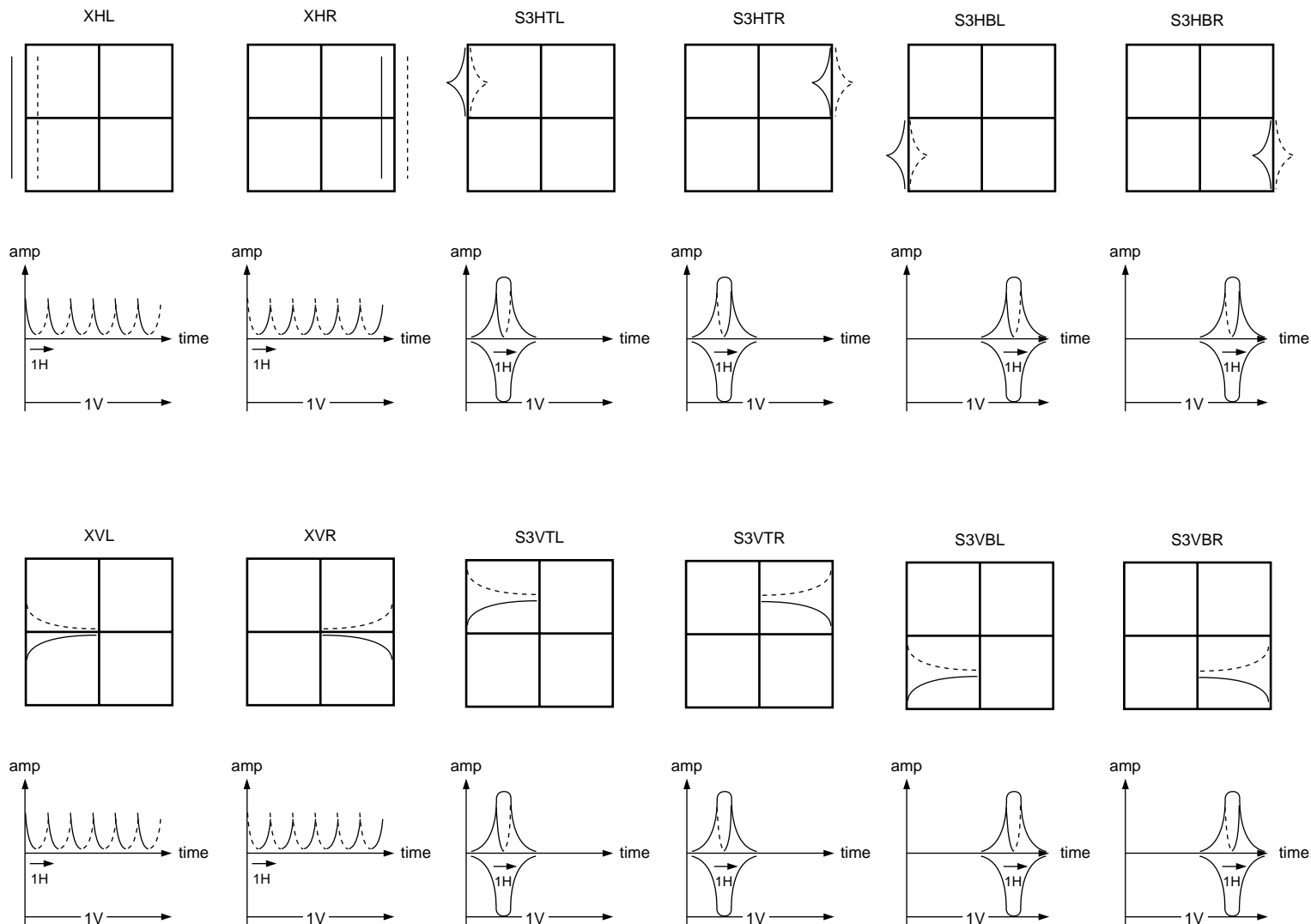
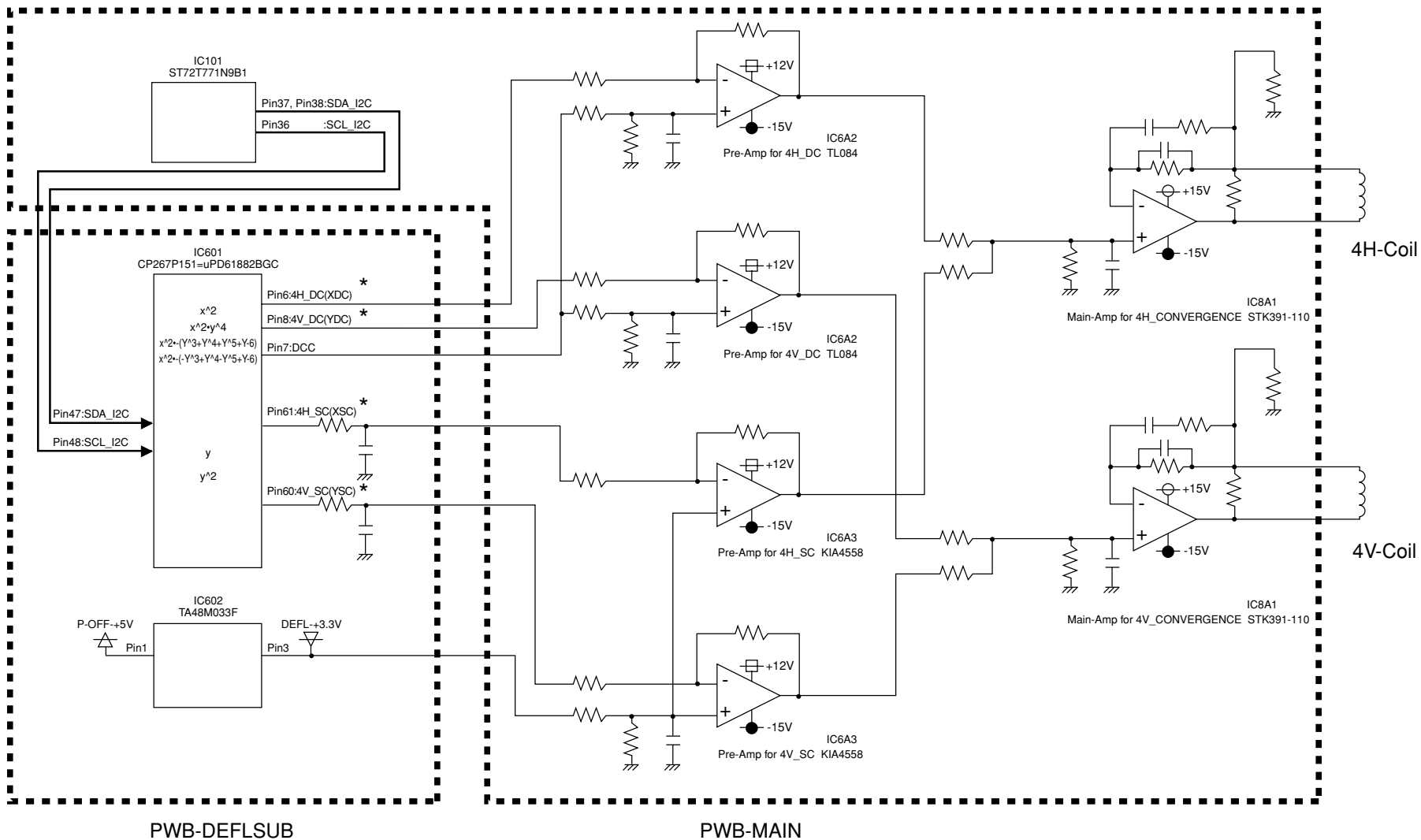


Figure 19 (b) DDC adjustment item

Figure 20 DDCC circuit diagram



★ Pin6:4H_DC(XDC) =XHL+XHR+S3HTL+S3HTR+S3HBL+S3HBR+PQH TL+PQHTR+PQHBL+PQHBR
Pin8:4V_DC(YDC) =XVL+XVR+S3VTL+S3VTR+S3VBL+S3VBR+PQVTL+PQVTR+PQVBL+PQVBR
Pin61:4H_SC(XSC) =H-CONVERGENCE • (YHTT+YHTB+YHJT+YHJB)
Pin60:4V_SC(YSC) =V-CONVERGENCE • (YVTT+YVTB+YVJT+YVJB)

1.6 Control block

The control block is composed of the following:

Monitor MPU IC101 to process the sync. signals, control the inside of the monitor and communicate with the external, EEPROM IC104 to memorize the picture adjustment values, I/O expander IC102 to output CS and V-LIN, etc.

1.6.1 Sync. signal process

When HSYNC or Composite Sync is input from the VIDEO board to the MPU IC101 pin 30 and VSYNC is input to the MPU IC101 pin 20 the frequency/polarity of SYNC will be discriminated. Then, HS_OUT will be output from pin 27 for beam deflection and OSD display and VS_OUT will be output from pin 26 as the polarity POSI.

If SYNC is not input or abnormal SYNC is input, the MPU IC101 will output simulative SYNC. The frequency of the simulative SYNC is near that of the previously input SYNC.

(Initial values: FH:31kHz and FV:60Hz)

1.6.2 Front button

When any tact switch of SW1X0 to SW1X8 on the front panel is pressed, the voltage of +5V will be divided with the resistor according to the button.

The signal is converted into the digital value with the A/D converter of the MPU IC101 pin 12 and pin 13 to discriminate which button is pressed.

1.6.3 I2C bus control

The IC control inside the monitor is carried out using pin 36: SCL-I2C, pin 37 and pin 38: SDA-I2C I2C bus.

The adjustment data corresponding to the input timing is read out from EEPROM and transmitted to each IC. For this I2C bus, the master always works as microcomputer. EEPROM IC104, deflection processor IC601, OSD-IC IC212, and pre-amplifier IC211 work as slaves, transmit control data. Each slave address is as mentioned in Table 6.

The MPU IC 101 pin 46 is a write protect signal of EEPROM IC 104. At normal state (when data is not written onto EEPROM), this signal is HI. When data is written onto EEPROM, this signal turns to LO.

With the SDA_I2C (input) of MPU IC 101 pins 37 and 38 turned to LO level for 2 seconds or more, the system regards the situation as I2C bus error, bringing the system forcibly to POWER SAVE state.

Table 6 Slave address list

Device	Symbol No.	ADR(HEX)
EEPROM	IC104	A0(Write) / A1(Read)
Deflection processor	IC601	DC
Preamplifier	IC211	78(Write) / 79(Read)
OSD	IC212	7A(Write) / 7B(Read)

1.6.4 Power control

The normal state and power management state are switched according to pin 33 P-OFF signal and pin 32 P-SUS signal.

"Power save" of the OSD adjustment item is turned to "ON", and the power management is activated when either H/VSYNC goes out.

In the power management mode, P-OFF+5V is turned OFF by setting pin 33 P-OFF signal at LOW, other power supplies except +5V and heater are turned OFF by setting pin 32 P-SUS signal at LOW.

Moreover, if pin 39 PRO 1 signal is at HI for 1 second or more, it will be regarded as a short circuit of the power of the secondary side to forcibly turn ON POWER SAVE in order to prevent trouble from being escalated.

1.6.5 ABL, Beam Protector

The feedback signal ABL of the beam current is input into MPU IC101 pin 16.

In case the signal ABL exceeds the voltage level given below, the contrast setting of the preamplifier IC211 is lowered down to prevent the excessive flow of the beam current.

ABL specified voltage: $\{5 * (\text{OSD item ABL}) / 256\}$ (V)

Further, in case the signal ABL exceeds the 4.7 V level continuously for 2 seconds or more, the situation is judged as circuit error, bringing the system forcibly to POWER SAVE mode.

1.6.6 CRT support

(1) Geomagnetism

The voltage conversion signal of horizontal magnetic field is output from pin 2 of the Geomagnetism sensor IC214, and the one of vertical magnetic field is output from pin 1 of the Geomagnetism sensor IC214. These are buffered or reversed and amplified by IC103 operational amplifier, and input to A/D converter of pins 18 and 19 of microcomputer IC101. These signals are converted to digital values, and the Geomagnetism around the monitor is detected.

(2) Temperature

The signal that divides the P_OFF_+5V at the thermistor TH100, R136 and R137 is input into the A/D converter of MPU IC101 pin 14 and converted into digital value. Thus, the temperature inside the monitor is detected.

(3) ON time

The monitor ON time signal BEAM TIME is input into the A/D converter of MPU IC101 pin 15 and converted into digital signal to detect the monitor ON time.

In order to cancel the deterioration in purity and convergence due to the aforesaid in (1) ~ (3) geomagnetism, temperature and variation with time, the cancel current is passed to each C_PURITY 4V coil.

Each C_PURITY ROTATION controls the PWM DAC output (pin 3 and pin 6 to pin 9) of MPU IC101 by means of the signal smoothened by R and C.

The digital signal transmitted to the deflection processor IC601 from the microcomputer through I2C bus and converted into analog voltage by IC601 is output from pin 60 then it controls the convergence 4V.

1.6.7 High voltage control

The high output voltage control is carried out by means of HV-ADJ signal smoothening the PWM DAC output of the microcomputer MPU IC101 pin 1 using R133 and C114.

The high voltage feedback signal X-PRO is input into the A/D converter of MPU IC101 pin 17. When this voltage exceeds the specified level for 600 msec or more, the situation is regarded as high voltage error, setting the monitor to POWER SAVE mode.

The specified voltage level is obtained from $\{5 * (\text{OSD item XPRO LEVEL}) / 256\}$ (V)

1.6.8 Display Data Channel

The DDC2B/2Bi function belongs to IC101 (microcomputer).

DDC2B: Immediately after the monitor power is turned ON, the microcomputer reads the EDID data from IC104. It outputs the EDID data according to the clock input into pin 34 SCL-DDC.

DDC2Bi: The monitor adjusts the picture etc. corresponding to DDC2Bi command which is input to pin 34 SCL-DDC and pin 35 SDA-DDC of microcomputer. This DDC2Bi command is used for the adjustment operated at factory. In case general user uses this, he/she needs specified application and adapter.

Table 7 IC101 (MPU) Pin assignment

PIN#	FUNCTION	ASSIGNMENT	PIN#	FUNCTION	ASSIGNMENT
1	DA0	H/V-ADJ(D/A)	56	VPP/TEST	GND
2	DA1	LIN(D/A)	55	IRIN	GND
3	DA2	ROTATION(D/A)	54	NOT(RESET)	RESET(IN)
4	DA3	VCANCEL(D/A)	53	PA0	SEL(OUT)
5	DA4	PWM-HEAT(D/A)	52	PA1	DATA(OUT)
6	DA5	TL(D/A)	51	PA2	CLOCK(OUT)
7	DA6	TR(D/A)	50	PA3	HSK(OUT)
8	DA7	BL(D/A)	49	PA4	USB-RST(OUT)
9	DA8	BR(D/A)	48	PA5	INT-SUB(OUT)
10	VSSA	GND	47	PA6	NC
11	VDDA	+5V	46	PA7/BLANKO	WP(OUT)
12	PB7/AN7	KEY-4DIR(A/D)	45	OSCIN	CRYSTAL-IN
13	PB6/AN6	KEY-PUSH(A/D)	44	OSCOUT	CRYSTAL-OUT
14	PB5/AN5	THERM(A/D)	43	USBVCC	NC
15	PB4/AN4	BEAM-TIME(A/D)	42	USBDP	NC
16	PB3/AN3	ABL(A/D)	41	USBDM	NC
17	PB2/AN2	X-PRO(A/D)	40	USBGND	GND
18	PB1/AN1	X-OUT(A/D)	39	PC7/TDO(SCI)	PRO1(IN)
19	PB0/VFBACK/AN0	Y-OUT(A/D)	38	PC6/RDI(SCI)	SDA-I2C(IN)
20	VSYNCI1	V-SYNC(IN)	37	PC5/SDAI(I2C)	SDA-I2C(OUT)
21	PC7/VSYNCI2/ITD	DEGAUSS(OUT)	36	PC4/SCLI(I2C)	SCL-I2C(OUT)
22	PD6/CLAMP0	CLP(OUT)	35	PC3/SDAD(DDC)	SDA-DDC(SIO)
23	PD5/ITA	LOCK(IN)	34	PC2/SCLD(DDC)/RX	SCL-DDC(SIO)
24	PD4/ITB	LED(OUT)	33	PCI/HSYNCI2	P-OFF(OUT)
25	PD3/ITC	SPARK(OUT)	32	PC0/OCMP/HFBACK	P-SUS(OUT)
26	PD2/VSYNCO	VS-OUT(OUT)	31	VDD	+5V
27	PD1/HSYNCO	HS-OUT(OUT)	30	HSYNCI1	H-SYNC(IN)
28	OD0/CSYNCI	G-SYNC(IN)	29	VSS	GND

1.6.9 Power-On Indicator

J100 pin 1 is connected to the anode of the green Power-On Indicator, J100 pin 3 is connected to the anode of the orange Power-On Indicator, and pin 2 is connected to the cathodes of both. Since P_OFF_+5V is normally supplied, the current flows to J100 pin 1 to turn OFF Q100.

Therefore, any current does not flow to J100 pin 3.

(The green Power-On Indicator only is lit.)

Since P_OFF_+5V is turned OFF in the power management mode, no current is not flowed to J100 pin 1 to turn ON Q100. Therefore, the current flows to J100 pin 3. (The orange Power-On Indicator only is lit.)

1.6.10 Clamp pulse

The clamp pulse signal CLP is output from pin 22 of the MPU IC101 with the polarity POSI. When "FRONT" is selected in the OSD adjustment item "CLAMP PULS POSITION", the signal is triggered at the front edge of HSYNC, and when "BACK" is selected, the signal is triggered at the rear edge.

1.6.11 SPARK

If it is electrically discharged in the CRT tube, the GND level of the high-voltage system circuit is considerably varied. GND of this high-voltage system is connected to the MPU IC101 pin 25 via C103. The voltage level of MPU IC101 pin 25 is normally set at HI. If GND in the high-voltage system varies since it is electrically discharged in the CRT tube, the current will flow to R130 to set MPU IC101 pin 25 at the LO level. Pin 25 is the external interrupt terminal that detects the trailing edge. When the trailing edge is detected, the MPU forcibly applies S/W RESET. (It is the same as when the power SW is turned ON.)

The above operation prevents the monitor from going out of control when it is electrically discharged in the CRT tube.

1.6.12 Avoidance operation during input SYNC switching

The horizontal LOCK output signal of the deflection processor IC601 pin 46 is connected to the MPU IC101 pin 23. MPU IC101 pin 23 is the external interrupt terminal of the trailing edge detection. Though the voltage level of the LOCK signal is normally set at HI, IC601 outputs LO when the horizontal deflection lock is released since the input SYNC is switched.

When the MPU detects the trailing edge, the HSK signal of IC101 pin 50 is set at HI, and the simulative SYNC that is near the original frequency is output from pin 26 and pin 27. HSK signal is used to set +B, voltage at MIN.

This reduces the stress when the input SYNC is switched for a short time.

1.6.13 CS switch and vertical linearity switch

Microcomputer IC101 outputs CS switch signal and vertical linearity switch signal via I/O expander IC102, and corrects the linearity in the screen.

Patterns of vertical linearity switch are shown in the table below.

As for CS switch pattern, refer to Table 4.

Table 8 SW_VLIN1, SW_VLIN2 select pattern (IC102)

Vertical frequency	SW-VLIN1 Pin 12	SW-VLIN2 Pin 13
50Hz ~ 77.9Hz	LO	LO
78Hz ~ 89.9Hz	HI	LO
90Hz ~ 124.9Hz	LO	HI
125Hz ~ 160Hz	HI	HI

1.6.14 H/W RESET

The +5V power is connected to pin 2 of the voltage detector IC100, and IC100 pin 1 output is connected to the MPU IC101 pin 54.

On the voltage detector, pin 1 is the open drain output, being turned OFF when pin 2 voltage is 4.5V or more, and ON when it is 4.5V or less. When the power switch is turned ON, IC100 pin 1 is turned ON and the MPU pin 54 level is set at 0V since +5V has not started up.

When the voltage of IC100 pin 2 becomes 4.5V or more, IC100 pin 1 will be turned OFF, and the voltage of the MPU pin 54 rises with the time constants of R100 and C100.

When the voltage of the MPU pin 54 becomes 3.5V or more, the MPU will start operating.

1.6.15 Oscillation circuit

The crystal oscillator X100 is connected to the MPU IC101 pin 45 and pin 44. Pin 45 is the clock input, and pin 44 is the amplification circuit output in the MPU. The operation frequency of the crystal oscillator is 24MHz. The basic clock is divided in the MPU to operate the program and circuits of the MPU.

1.6.16 I/O expander

Pin 51 CLOCK and pin 52 DATA of microcomputer are a serial interface for transmit the output data to I/O expander IC102. I/O expander inside is a shift register, and interface only transmits the data to this shift register in order and sends the latch signal.

1.7 Software

1.7.1 Outline

(1) Input frequency

- Horizontal : 30kHz to 121kHz (Lower limit : 29.5kHz, Upper limit: 125kHz)
- Vertical : 50Hz to 160Hz (Lower limit: 47Hz Upper limit: 162Hz)

(2) Memory timing number

- Preset timing : 10 timing (22 timing max.)
- User timing : 15 timings can be memorized.

1.7.2 Frequency variation detection function

At normal signal input, this function checks the input frequency and polarity per VSYNC input and judges that input signal has been transmitted if the conditions a, b and c given below are satisfied 4 times continuously against the first synchronous signal state.

Condition a: There is no change in the input synchronous signal polarity both in horizontal and vertical directions.

Condition b: The horizontal frequency difference is less than 0.4kHz.

Condition c: The vertical frequency difference is less than 0.4Hz.

On detecting the change in input signal, this function compares, in the order given below, the directory data written in EEPROM with the directory data of the input signal before reading and outputting the screen data.

(1) If the input signals satisfy conditions a, b and c, they are judged to be the same as the signals registered in the directory, and the timing data are read from EEPROM and are output.

Condition a: The polarities of the input sync. signal are the same in both horizontal and vertical directions.

Condition b: Horizontal frequency difference is 0.6kHz

Condition c: Vertical frequency difference is 0.6Hz.

The sequence of the compared directories is as follows:

PRESET1 → PRESET2 → ... → PRESET10 → USER1 → USER2 → ... → USER15

If the same timing is judged on the way, the comparison work is stopped there, and the adjustment value for each corresponding timing is read out from EEPROM.

(2) If the conditions of (1) are not satisfied (when the new timing is input), the horizontal frequency reads the backup picture data of the nearest preset timing and outputs it.

1.7.3 Memory of user timing

The new timing is input. When the picture adjustment is executed, the directory data (frequency and polarity) and picture data will be memorized in EEPROM.

If 15 user timings (MAX) are memorized, the memory of the oldest user timing (directory data and picture data) is deleted, and the new timing information is memorized there.

USER1 → USER2 → ... → USER15 → USER1 → USER2 → ... →

1.7.4 Picture adjustment

- (1) The monitor has the function to do the picture adjustment with OSD and communication.

The function has the following adjustment modes.

a: Normal mode

b: Factory mode

For entry into each adjustment mode, refer to Item "Adjustment method".

- (2) High voltage adjustment supplement

High voltage under normal conditions is decided by "HVAD" setting value of OSD adjustment item, and X-ray protect voltage is decided by "XPRO" setting value of OSD adjustment item. For X-ray protect voltage, the calculated value is set inside the microcomputer by executing XPRO CALIBRATE with the input frequency 32kHz or less.

- (3) If XRAY-PROTECT activates even in the normal state because XRAY-PROTECT is excessively lowered by mistake, the XRAY-PROTECT and HV-ADJUST adjustment values can be initialized using the following procedure.

(a) Input the image signal to the monitor.

(b) Keeping both + and - buttons pressed, turn ON the power.

(c) Keep both + and - buttons pressed for approx. 30 seconds or more.

(d) Release - button only.

(e) Keep the + button only pressed for 15 seconds or more.

(f) When it is successfully completed, Power-On Indicator gets green in a flash.

(g) Turn OFF the power, and turn it ON again, and the XRAY-PROTECT adjustment value will become 254 and HV-ADJUST adjustment value will become 0.

- (4) Vertical position adjustment supplement

The displayed adjustment data corresponding to the vertical position icon in OSD adjustment item differs at Normal and Factory mode.

Normal mode ("VERT-POSITION"):

When this icon is moved, the trapezoid distortion compensation is automatically carried out. This is mainly used for compensating the distortion against the vertical position of the input timing image.

Factory mode ("PF"):

The trapezoid distortion compensation is not carried out automatically even if this icon is moved. This is mainly used for compensating the offset of the circuit and deflection yoke.

1.7.5 Power management

The function reduces the power consumption of the monitor when the connected computer is not used.

The function is turned ON and OFF from the adjustment picture.

The monitor has only one kind of the power management function.

- (1) Conditions to enter power management mode

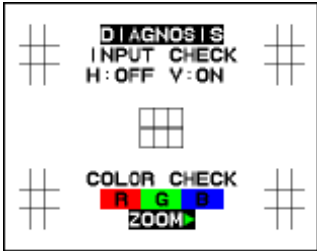
a: "POWER SAVE" of the picture adjustment item is left ON.

b: Neither HSYNC nor VSYNC are input.

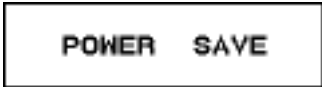
- (2) Power management operation
- When the power management is activated,
- (i) P_SUS signal is turned to LO to stop the power output on the secondary side except CRT heater, P-OFF+5V, +5V line.
 - (ii) P-OFF signal is turned to LO to stop the power output of P-OFF+5V line.
 - (iii) The front Power-On Indicator is lit orange.

1.7.6 OSD display at NO SYNC

- (1) In case there is no input in either HSYNC or VSYNC, the following OSD is displayed.
- (a) When OSD item "POWER SAVE" is set to "OFF", this OSD is continuously displayed.
 - (b) When OSD item "POWER SAVE" is set to "ON", this OSD is displayed for about 6 sec and moves to (2)

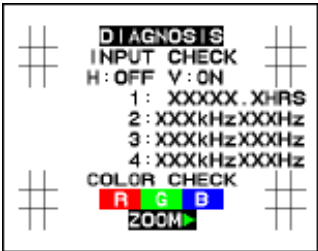


- (2) After displaying the OSD given below for about 3 seconds, the system enters POWER MANAGEMENT mode.



- (3) During POWER MANAGEMENT mode, if one of the buttons is pressed, the OSD in (1) is displayed again.
- If no button is further pressed, the display moves to the state in (2) after about 1 minute.
- (4) If "→" button is pressed with OSD in (1) under display, cross hatch is displayed in the back of OSD. If "→" is pressed again, it returns to the initial screen.

- (5) If "-" and "+" buttons are simultaneously pressed with OSD in (1) under display, the OSD given below is displayed. If no button is pressed for about 1 minute, the displays from 1: to 4: are deleted.



- * Item 1: Operating time (Cumulative time while the power switch is ON)
- Item 2: Preceding input frequency, horizontal frequency, and vertical frequency
- Item 3: Input frequency, horizontal frequency, and vertical frequency before item 2
- Item 4: Input frequency, horizontal frequency, and vertical frequency before item 3

1.7.7 Power-On Indicator display

Normally Power-On Indicator is lit up green during screen display and orange during power management.

However, when circuit operation error is detected, the system gets forcibly set to POWER MANAGEMENT mode, with Power-On Indicator being lit up in the pattern given below.

	Power-On Indicator Indication
High voltage protector action	<div> <div></div> <div></div> <div></div> <div></div> </div>
High voltage adjustment data error	<div> <div></div> <div></div> <div></div> <div></div> <div></div> <div></div> </div>
Beam protector action	<div> <div></div> <div></div> <div></div> <div></div> <div></div> <div></div> <div></div> <div></div> </div>
Secondary side load short-circuit	<div> <div></div> <div></div> <div></div> <div></div> <div></div> <div></div> <div></div> <div></div> <div></div> <div></div> </div>

- : Orange ON (1sec)
- : Power-On Indicator OFF (1sec)
- : Orange ON (4sec)

* EEPROM memory error: Each of the high voltage adjustment “HVADJ” and “XPRO LEVEL” has independent backup data. As the power is turned ON, each adjusted value is read from EEPROM, and in case this value fails to correspond with the backup data, the situation is regarded as EEPROM memory error, setting the system forcibly to POWER MANAGEMENT mode.

1.7.8 Status memory to EEPROM

The following contents are stored in EEPROM in order to supplement the analysis of fault and claim causes.

(1) Operation time/Heater ON time

Operation time: Total time that the power supply switch is ON, Heater ON time: Total time that HEATER voltage is ON, both are by 30 min. unit, and memorized in EEPROM by 2 byte in size. When the memory value becomes FFFFH, count up stops. Item 1 of OSD indication in 1.7.6-(5) shows this memory value.

Table 9

EEPROM address	Content
0 x 0A0	Lower byte of operation time
0 x 0A1	Upper byte of operation time
0 x 0A3	Lower byte of HEATER ON time
0 x 0A4	Upper byte of HEATER ON time

(2) Operating frequency memory

The input frequency for the past 3 times is memorized in EEPROM in 2*3 byte size.

The items 2 to 3 of OSD display in 1.7.6-(5) display these memory values.

In case the input frequency exceeds 3 times, the oldest memory value is discarded.

Table 10

EEPROM address	Content
06C	Preceding input horizontal frequency (unit: kHz)
06D	Preceding input vertical frequency (unit: Hz)
06E	Input horizontal frequency one step before (unit: kHz)
06F	Input vertical frequency one step before (unit: Hz)
070	Input horizontal frequency two steps before (unit: kHz)
071	Input vertical frequency two steps before (unit: Hz)

(3) Protector operation rate memory

The protector operation rate due to error in high voltage, power short-circuit on the secondary side, BEAM, high voltage false, or EEPROM is memorized in EEPROM in 6 byte size. The data is memorized in EEPROM per FACTORY ADJUSTMENT and USER mode (total 12 byte).

1.8 Deflection processor block

1.8.1 Outline

The deflection processor block mainly composed of deflection processor IC generates and controls a variety of the following compensation waveform that are produced by this IC.

The deflection processor IC is a 64pins IC of uPD61882 of IC601.

The following seven points are generated and controlled by the deflection processor IC.

(Refer to the block diagram of IC601 in the figure 21.)

- (1)Vertical deflection waveform generating circuit
- (2)Horizontal deflection drive waveform generating circuit
- (3)Distortion compensation waveform generating circuit
- (4)DBF compensation waveform generating circuit
- (5)Convergence compensation waveform generating circuit
- (6)Blanking waveform generating circuit
- (7)Moire canceling circuit

Moreover, the block is provided with a small both-face board (PWB-DEFL-SUB) of 60mm X 70mm.

The power of the deflection processor block is +3.3V that is converted from P-OFF+5V by the regulator of IC602, and the power and GND are divided into the digital system and analog system in the inner circuit of IC601 in order to prevent noise interference for the waveforms.

OP amplifier of IC603 uses the power of +5V and -15V, and works as the trace filter and voltage amplification of the amplitude of the saw-toothed waveform for vertical deflection.

1.8.2 Vertical deflection waveform generating circuit

The deflection processor IC (IC601) does 10-bit DAC output of the saw-toothed wave for vertical deflection that is synchronized with the vertical frequency input to pin 42, from pin 1 and pin 11 at both polarities (approx. 1.2V.p-p). Moreover, the center voltage IMID (approx. 1.6VDC) of the saw-toothed wave is output from pin 2.

To remove the noise, the OP amplifier (pins 1, 2 and 3) of the front step of IC603 removes the difference between the waveforms of both polarities of the saw-toothed wave for vertical deflection, using the center voltage IMID of the saw-toothed wave as the reference. From the output of the amplifier, the digital gradation component of the saw-toothed wave is removed with the low pass filter that is made of R642 and C628. Moreover, pin 62 and pin 63 of IC601 are the analog switch turning ON the retrace term, prevents the waveform deformation that is produced by the low pass filter, and prevents the degradation of the linearity and the fluctuation of the scanning line.

Moreover, the saw-toothed wave for vertical deflection is controlled to adjust the vertical picture width, vertical phase and linearity.

R645, R646, R647 and R649 connected to pair GND on the filter output composed of R642 and C628 are the resistor to improve the linearity of the saw-toothed wave for input vertical deflection, and switches the resistance into four steps with the transistor switch of Q603 and Q604 according to the vertical frequency. (Refer to Table 12.)

The saw-toothed wave for vertical deflection is output to the low output impedance with the OP amplifier (pins 5, 6 and 7) of the rear step of IC603.

Vertical frequency	Q604	Q603
50 ~ 77.9Hz	OFF	OFF
78 ~ 89.9Hz	ON	OFF
90 ~ 124.9Hz	OFF	ON
125 ~ 160Hz	ON	ON

Table 12 Vertical linearity compensation resistance select transistor ON/OFF

1.8.3 Horizontal deflection drive waveform generating circuit

The rectangular wave for horizontal deflection drive are output at the amplitude 3.3Vp-p and approx. 45% Duty from IC601 pin 25 with the delay of the transistor taken into account in order to make the Duty become 50% at the output of Q501 of the horizontal deflection circuit.

Here, the simulative horizontal sync. signal (5V pulse) from the horizontal flyback pulse (AFC, 5V pulse) input to IC601 pin 27 and IC101 (MPU) input to IC601 pin 44 is passed through the inverter of IC6A1 to produce the edges of these waveforms. This prevents the noises of the jitter, etc. from generating.

Moreover, the circuit composed of Q602, Q605, etc. connected to IC601 pin 13 prevents the rapid frequency variation of the horizontal output when the horizontal input signal becomes no signal. IC601 pin 13 is a phase comparator filter terminal to phase-lock the horizontal input sync. signal and the oscillation in IC601. When the horizontal input sync. signal becomes no signal, the terminal voltage rapidly varies from approx. 0.8V of the phase lock time to 0V, and the frequency of the horizontal output rapidly varies according to this. The circuit is added to compress the rapid frequency variation width by smoothening the variation of the terminal voltage of pin 13 by C636 when it becomes unlocked. This prevents the horizontal collector pulse from jumping in order to prevent overvoltage against the horizontal output transistor (Q502).

The terminals pin 13 to pin 20 of IC601 become the control filter terminal of horizontal PLL.

1.8.4 Distortion compensation waveform generating circuit

The deflection distortion compensating waveform is output from pin 64 of IC601. The waveform is output from 1-bit DAC, and 3.3V pulse waveform of resolution power of 25MHz is output at pin64 direct. The pulse waveform is smoothened with the low pass filter of R632 and C622 to gain the compensation waveform of the vertical frequency. The amplitude is approximately 1.0 to 1.2Vp-p, and is connected to pin5 of IC5J1.

The horizontal size, trapezoid compensation, side pin compensation, upper/lower compensation of the side pin, S type compensation of the side pin and W compensation of the side pin are applied. (Refer to the compensation image, figure 22.)

The deflection compensation waveform in the horizontal phase system is output from pin 57 of IC601. Pin 57 is the 1-bit DAC output, and outputs the pulse waveform of 3.3V of resolution power of 25MHz. The pulse waveform is smoothened with the low pass filter of R614, R619, C601 and C604, and the waveform of the vertical frequency is current-added to the filter (pin 20 of IC700) of the horizontal system PLL to compensate for the deflection distortion of the horizontal phase system. The parallel rectangular distortion compensation and the side pin balance (upper and lower) compensation are executed. (Refer to the compensation image, figure 22.)

1.8.5 DBF compensation waveform generating circuit

The horizontal system DBF compensation waveform is output in 8-bit DAC mode from pin 10 of IC601. The amplitude is approximately 0.5Vp-p. It is connected to pin 6 of IC6A2.

The vertical system DBF compensation waveform is output from pin58 in the 1-bit DAC mode. Pin 58 direct outputs the pulse waveform of the resolution power of 25MHz. The pulse waveform is smoothened with the low pass filter of R621 and C607 to gain the DBF compensation waveform of the vertical frequency. The amplitude is approximately 0.6Vp-p. It is connected to pin 3 of IC6A2.

1.8.6 Convergence compensation waveform generating circuit

The horizontal dynamic convergence compensation waveform is output from pin 6 of IC601 in the 8-bit DAC mode. The amplitude is approximately 0V to 0.5V. The vertical dynamic convergence compensation waveform is output from pin 8 in the 10-bit DAC mode. The amplitude is approximately 0V to 0.5V. The dynamic convergence compensation waveform center voltage (approx. 1.6V) is output from pin 7.

In the 1-bit DAC mode, the horizontal static convergence compensation waveform is output from pin 61, and the vertical static convergence compensation waveform is output from pin 60. In pins 60 and 61 direct, the pulse waveform of the resolution power of 25MHz is output. The pulse waveform is smoothened through the low pass filter to gain the horizontal static convergence compensation waveform and vertical static convergence compensation waveform of the vertical frequency.

1.8.7 Blanking waveform generating circuit

The horizontal blanking pulse and vertical blanking pulse are generated in IC601, and these two waveforms are mixed and output at 3.3Vp-p from pin 40 of IC601.

The reference of the phase of the vertical blanking pulse is determined at the leading edge of VFLY (vertical flyback pulse, 5V pulse) of pin 39 input of IC601, and the phase can be variably controlled to output the optimal waveform of the blanking pulse.

The horizontal blanking pulse is a pulse that is synchronized with H-IN (horizontal sync. signal, 5V pulse) of pin 44 input of IC601, and can be also variably controlled.

The waveform is connected to pin 6 of the preamplifier (IC211) of the video board.

1.8.8 Moire canceling circuit

The moire canceling circuit outputs the waveform that is reversed every line of the horizontal frequency and every 1 frame of the vertical frequency from pin 22. The vertical frequency waveform is output from pin 23, and these two waveforms are added to the horizontal PLL through the filter of R630 and C618 to achieve the moire canceling function.

Pin 30 of IC601 is a terminal to detect the drop of the power voltage (+3.3V), and the detection voltage is approximately 1.0V. When a power voltage drop is detected, pin 32 of IC601 varies from Hi level (5V) to Lo level (0V) but is not used now.

Pin 46 is a terminal to detect whether the horizontal PLL is locked and HD output from pin 25 is normal or not. It is output at the Hi level (5V) when it is locked, and at the Lo level (0V) when it is unlocked. It is connected to IC103 (MPU).

Pin 49 is the reset terminal of IC601. The reset IC of IC6A4 resets IC601 when P-OFF+5V drops to approx. 2.7V.

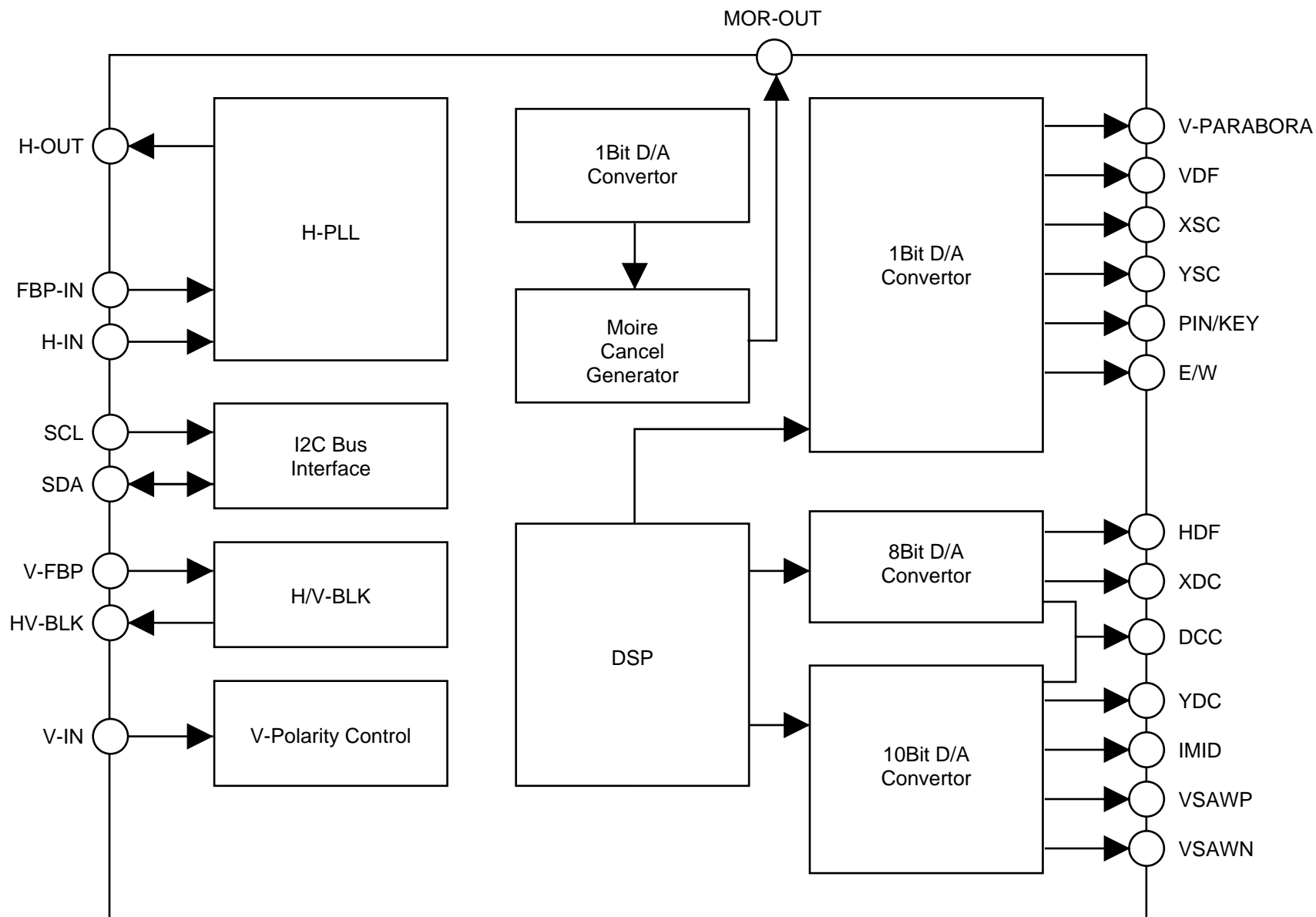
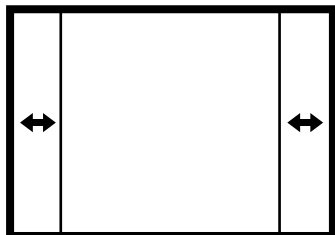


Figure 21 IC601 block diagram (uPD61882BGC)

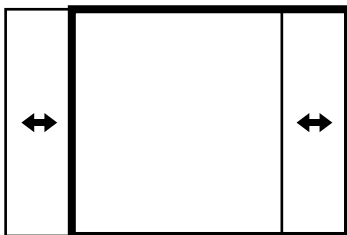
1.8.9 Distortion compensating operation

The followings are the operation image figures on the picture of the distortion compensation.

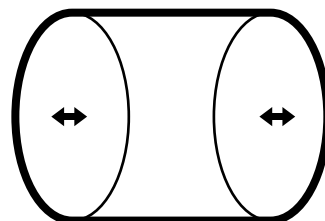
HORIZE-SIZE



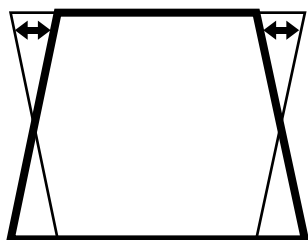
HORIZE-PHASE



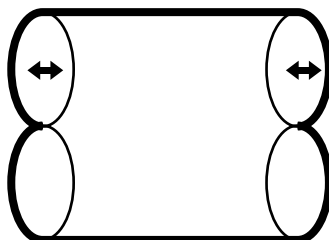
PINCUSHION



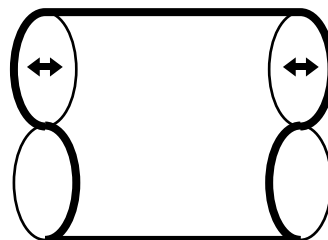
KEYSTONE



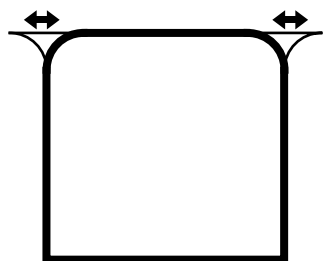
PIN-CENTER



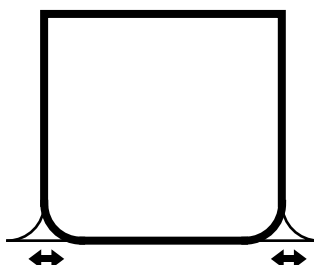
PCC-SINE



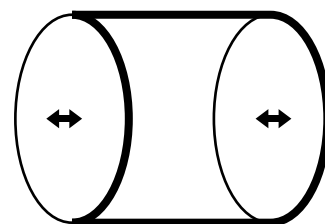
TOP-PIN



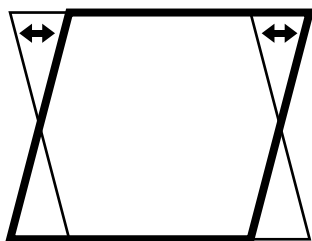
BOTTOM-PIN



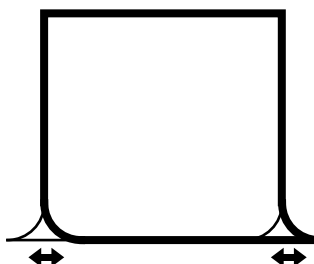
PIN-BALANCE



KEYBALANCE



BOTTOM-PIN



TOP-PIN

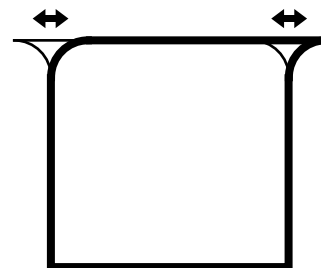


Figure. 22

1.9 Video Block

1.9.1 Picture signal amplifier circuit

As for picture signal (video) amplification circuit, R, G and B is respectively the same circuit in structure. G (green) video circuit is explained in this section.

There are two systems, i.e. SIGNAL-A and SIGNAL-B, in the video input terminal, and both have a D-SUB connector.

SIGNAL-A input means to input from pin 2 of D-SUB connector J215 to pin 12 of analog switch IC216.

SIGNAL-B input means to input from pin 2 of D-SUB connector J216 to pin 4 of analog switch IC216.

(Refer to A point.)

Analog switch IC216 selects the signal when SIGNAL-A and SIGNAL-B are simultaneously input.

As for the method of selecting the signal, according to SELECT signal of pin 53 of microcomputer IC101, input signal SIGNAL-A is selected when pin 13 of analog switch IC216 (SELECT SW) is HIGH, and input signal SIGNAL-B is selected (refer to B point) when it is LOW. Either signal is output from pin 28 of analog switch IC216.

Video signal output from pin 28 of analog switch IC216 is input to pin 10 of Pre-AMP IC211. (Refer to C point.)

For video signal, voltage amplification, composite and amplitude control [Explanation 1] is performed in Pre-AMP IC211, and the signal is output from pin 27. (Refer to D point.)

Video signal output from Pre-AMP is input to pin 8 of MAIN-AMP IC210 and is output from pin 5 of MAIN-AMP IC210 after final amplification. (Refer to E point.)

(MAIN-AMP IC210 is an amplifier to amplify the video signal with voltage (GAIN: 12 to 15 times).

The video signal is coupled by AC to cut-off circuit (Refer to the cut-off circuit mentioned below.), and then it is input to CRT socket J200 via connector J202 on CRT substrate through connector J210, and supplied to the cathode of CRT. (Refer to F point.)

[Explanation 1] Duty of Pre-AMP IC211

- Voltage amplification of video signal (GAIN: 0 to 5 times)
- Composite of the video signal for adjustment screen (OSD) output from IC212 and the blanking signal output from IC601
- Amplitude control of output voltage (ABL control) <Note 1>
- D/A output for bias control

The above is completely controlled by I2C bus (IC211 pin 3: SDA_I2C, pin 4:SCL_I2C) comes from microcomputer IC101.

<Note 1>

According to detection of current by the flyback transformer on MAIN substrate, the upper limit value of brightness when the screen is totally white, by controlling CRT anode current.

1.9.2 Cut-off circuit

The video signal amplified with voltage in the picture signal amplification circuit is coupled by AC (superimpose the pulse into DC voltage) to the cut-off (diode clamp) circuit (DC bias control circuit) consists of D250G, D251D, Q250G and Q251G at C210G.

The cut-off (DC bias control) circuit changes back raster brightness and chromaticity (bias) by brightness control signal and bias control signal.

The brightness control signal, which is superimposing SUB-BRT signal (for factory adjustment) output from pins 14 and 13 of OSD-IC IC212 and BRT signal (for user adjustment) output from pin 32 of Pre-AMP IC211 at OP-AMP IC213, is output from pin 1 of OP-AMP IC213. When the superimposed brightness control signal is applied to the emitter of the base ground transistor Q250G, the back raster brightness changes.

The bias control signal is output from pin 30 of Pre-AMP IC211. The bias control signal is, as well as the brightness control signal, applied to the emitter of the base ground transistor Q250G, and changes the back raster chromaticity (BIAS).

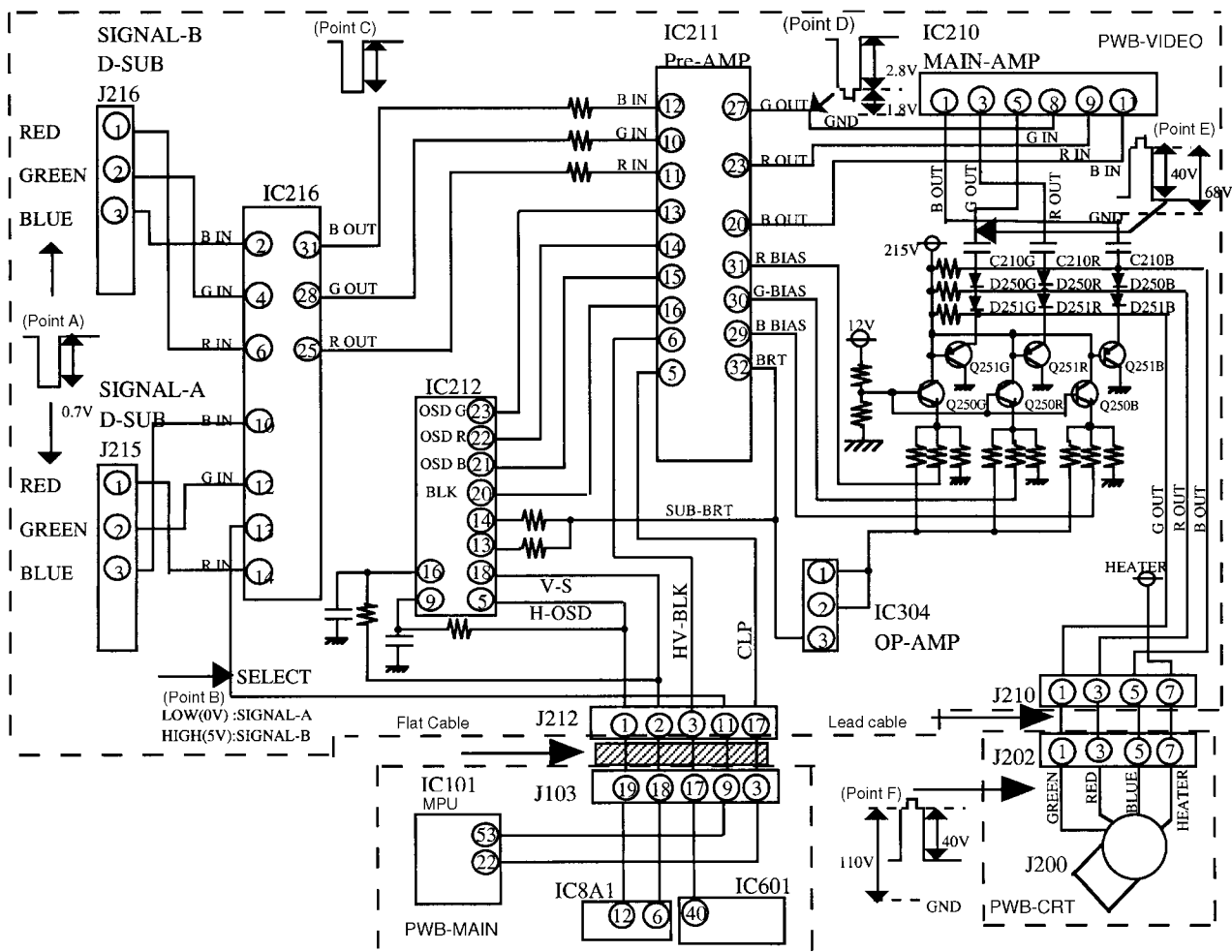
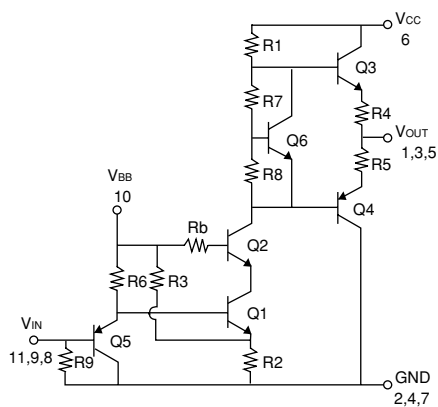
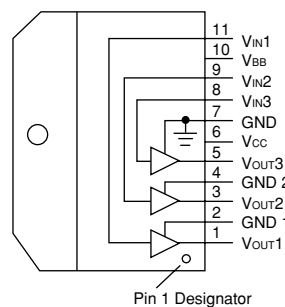


Figure 23 Video signal amplification circuit diagram



Simplified Schematic Diagram
(One Channel)



Top View

Figure 24 IC210 (LM2402T) block diagram

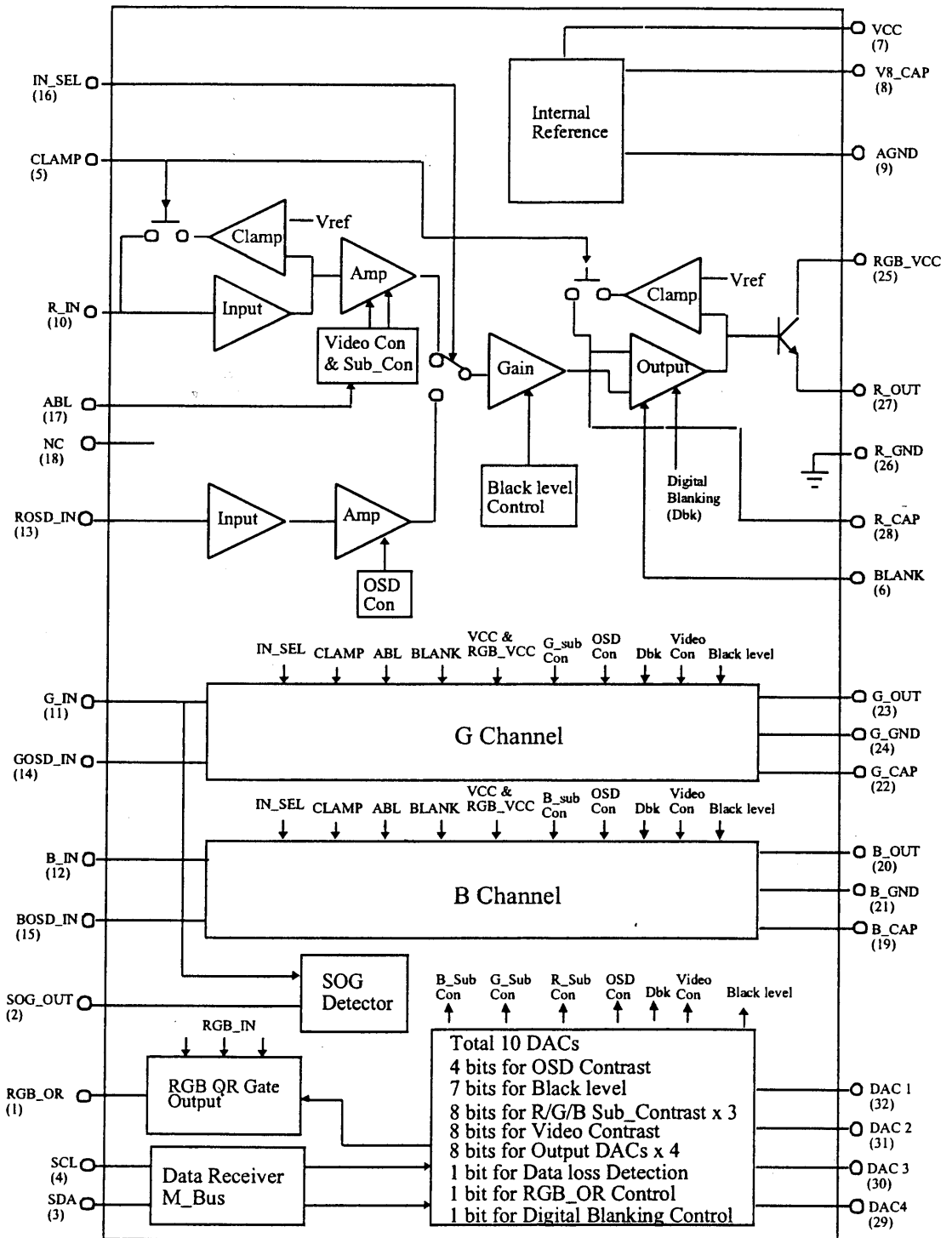


Figure 25 IC211 (MC13289ASP) block diagram

1.9.3 2-input change over circuit and synchronizing signal circuit

There are two systems; SINGAL-A and SIGNAL-B, as well as the video input terminal, in synchronizing signal input terminal, and both has a D-SUB connector. Since input terminals and circuit operation are different in each synchronizing signal (separate, composite, picture composite), each synchronizing signal is explained in this section.

[Separate synchronizing signal] (Separate Sync)

Horizontal synchronizing signal which has been input from SINGAL-A is input from pin 13 of D-SUB connector J215 to pin 15 of analog switch IC216, and the vertical synchronizing signal is input from pin 14 of D-SUB connector J215 to pin 16 of analog switch IC216. Besides, the horizontal synchronizing signal which has been input from SINGAL-B is input from pin 13 of D-SUB connector J216 to pin 7 of analog switch IC216, and the vertical synchronizing signal is input from pin 14 of D-SUB connector J216 to pin 8 of analog switch IC216. (Refer to A point.) The analog switch IC216 selects a signal (2-input change over) when SIGNAL-A and SIGNAL-B are simultaneously input, as well as the video signal.

As for the method of selecting a signal, like the video signal, according to SELECT signal of pin 53 of microcomputer IC101, input signal of SIGNAL-A is selected when pin 13 of analog switch IC216 (SELECE SW) is HIGH, and input signal SIGNAL-B is selected (refer to B point) when it is LOW. They are output from pin 19 (horizontal synchronizing signal) and from pin 18 (vertical synchronizing signal) of analog switch IC216. (Refer to C point.)

The horizontal synchronizing signal and vertical synchronizing signal, which are output from analog switch IC216, are supplied to pin 30 (H-SYNC) and to pin 20 (V-SYNC) of microcomputer IC101 on PWB-MAIN via the flat cable, respectively.

As for the polarity of the separate synchronizing signal, there are the positive polarity (POS) and the negative polarity (NEG). The following Fig. 26 shows the case that the positive polarity (POS) is input.

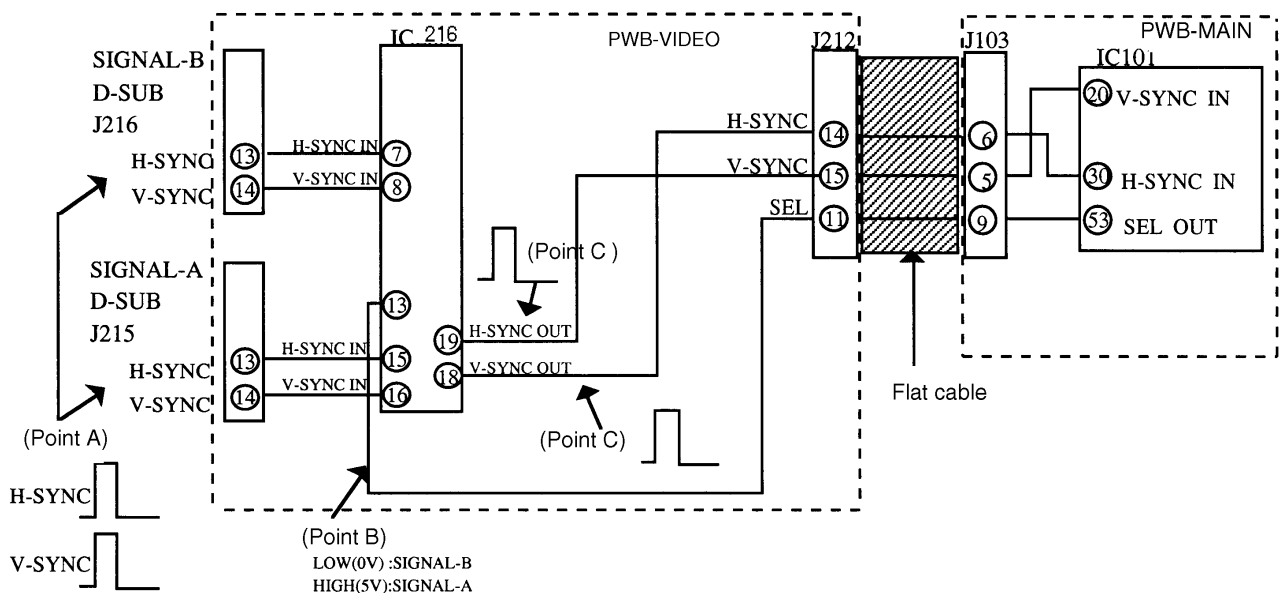


Figure 26 2-input change over circuit and separate synchronizing signal

[Composite synchronizing signal] (Composite Sync)

The composite synchronizing signal which has been input from SINGAL-A is input from pin 13 of D-SUB connector J215 to pin 15 of analog switch IC216. While, the composite synchronizing signal which has been input from SINGAL-B is input from pin 13 of D-SUB connector J216 to pin 7 of analog switch IC216. (Refer to A point.)

Analog switch IC216 selects a signal (2-input change over) when SIGNAL-A and SIGNAL-B are simultaneously input, as well as the separate synchronizing signal.

As for the method of selecting a signal, like the separate synchronizing signal, according to SELECT signal of pin 53 of microcomputer IC101, the input signal of SIGNAL-A is selected when pin 13 (SELECE SW) of analog switch IC216 is HIGH, and the input signal SIGNAL-B is selected (refer to B point) when it is LOW. Either signal is output from pin 19 of analog switch IC200. (Refer to C point.)

The composite synchronizing signal output from analog switch IC216 is supplied to pin 30 of microcomputer IC101 on PWB-MAIN via the flat cable, and its synchronization is separated at microcomputer IC101.

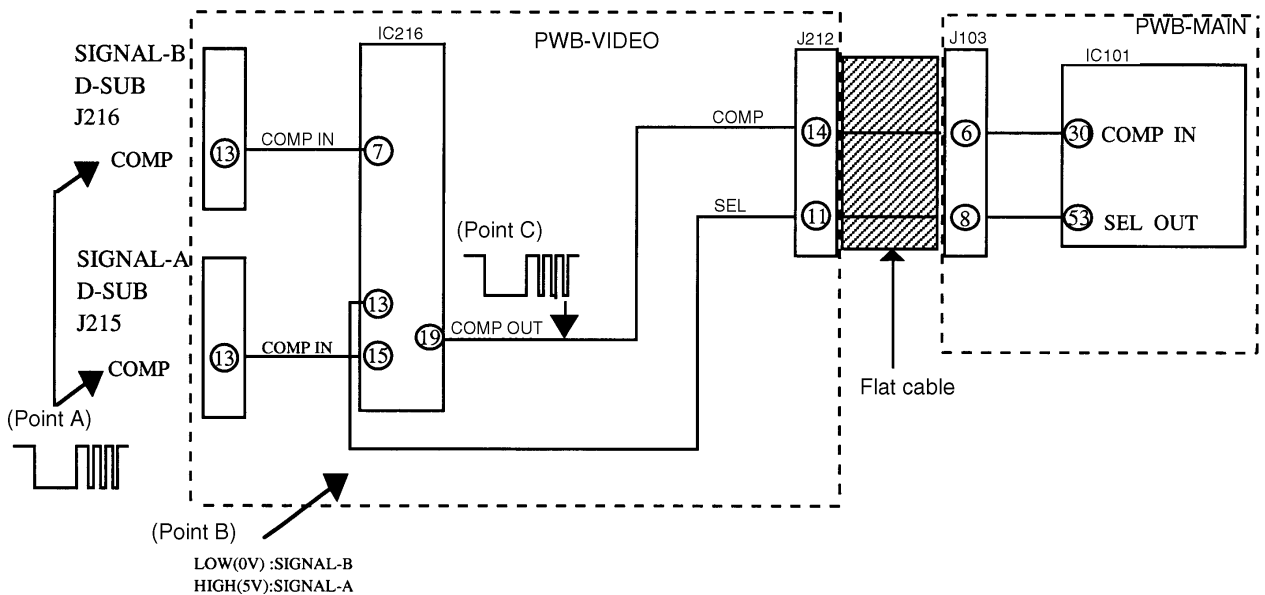


Figure 27 2-input change over circuit and composite synchronizing signal

[Picture composite synchronizing signal] (Sync on Green)

The picture (green video) composite synchronizing signal, which has been input from SIGNAL-A, is input from pin 2 of D-SUB connector J215 to pin 12 of analog switch IC216. While, the picture (green video) composite synchronizing signal, which has been input from SIGNAL-B, is input from pin 2 of D-SUB connector J216 to pin 4 of analog switch IC216. (Refer to A point)

Analog switch IC216 selects a signal (2-input change over) when SIGNAL-A and SIGNAL-B are simultaneously input, as well as the separate synchronizing signal and the composite synchronizing signal.

As for the method of selecting a signal, like the separate synchronizing signal and the composite synchronizing signal, according to SELECT signal of pin 53 of microcomputer IC101, the input signal of SIGNAL-A is selected when pin 13 of analog switch IC216 (SELECE SW) is HIGH, and the input signal SIGNAL-B is selected (refer to B point) when it is LOW. The video signal is output from pin 28 (refer to C point), and the composite synchronizing signal (refer to D point) is output from pin 21 of analog switch IC216.

For the picture composite synchronizing signal, it is necessary to separate it to a video signal and a composite synchronizing signal.

The picture composite synchronizing signal is separated to a picture signal and a composite synchronizing signal as follows.

When microcomputer IC101 detects the picture (green video) composite synchronizing signal, S/G-SEL signal of microcomputer IC101 becomes HIGH (5V), transistor Q280 turns OFF, the picture (green video) composite synchronizing signal is output from pin 23 of analog switch IC216. The picture (green video) composite synchronizing signal, which is output from pin 23, is input to pin 22 of analog switch IC216.

Then, after it is separated to a picture signal and a composite synchronizing signal in analog switch IC216, the composite synchronizing signal only is output from pin 21.

The composite synchronizing signal which has been output from pin 21 of analog switch IC216 is supplied to pin 28 of microcomputer IC101 on PWB-MAIN via the flat cable, and its synchronization is separated in microcomputer IC101.

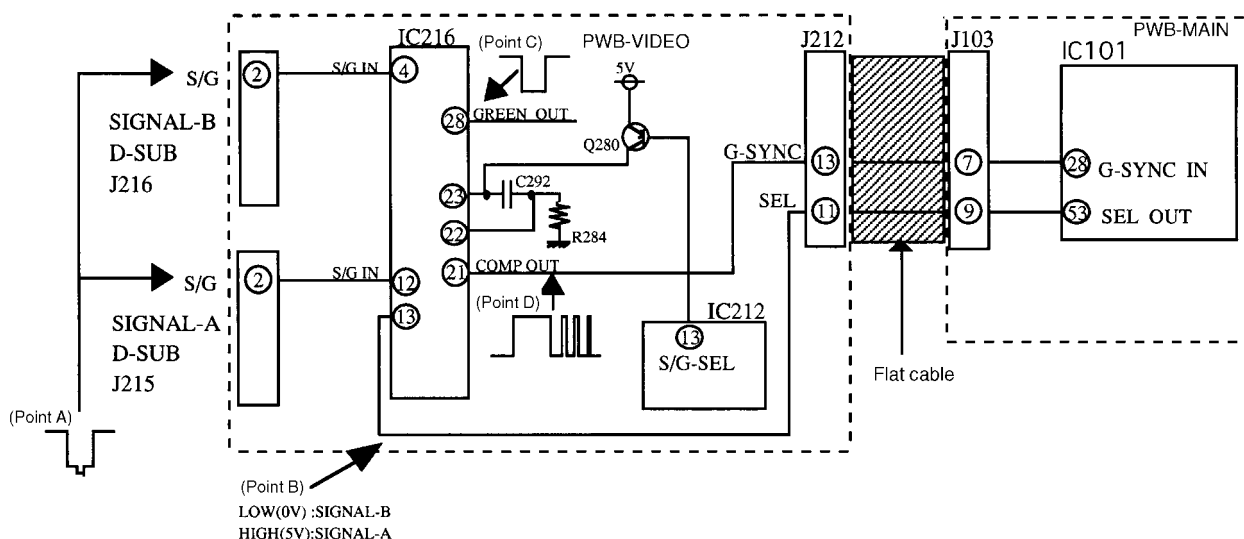


Figure 28 2-input change over circuit and picture composite synchronizing signal

1.9.4 On screen display circuit

The control signal on adjustment screen (OSD) is input to pin 8 (CLK), pin 7 (DATA), pin 5 (H-BLK) and pin 18 (V-BLK) of IC212.

IC212 outputs the signals from pin 20 (BLK), pin 21 (OSD-B), pin 22 (OSD-R) and pin 23 (OSD-G), and they are composed with the video signal at IC211.

1.9.5 AUTO-SIZE function

AUTO-SIZE functions to calculate the required width and position of screen in user mode based on the position of picture signal and the phase of AFC Feed Back and to automatically adjust them. "AUTO SIZE ADJUST" is selected in OSD, and when (+) button is pressed, AUTO SIZE ADJUST process is operated.

<AUTO-SIZE circuit action>

AUTO-SIZE detects the phase data of RGB OR signal, which is output from Pre-AMP IC211 to OSD-IC IC212, based on H-OSD and V-S signals input to OSD-IC IC212. Then, it sends the data to microcomputer IC101 via I2C bus so as to be calculated and processed.

The details are as follows.

RGB OR signal output from pin 1 of Pre-AMP IC211 is input to pin 19 of OSD-IC IC212. (C point)
H-OSD signal output from pin 12 of inverter IC8A1 on PWB-MAIN is input to pin 5 (B point) of OSD-IC IC212 via connector J212 on PWB-VIDEO from connector J103, and the signal (A point) with delay of 700ns by filters of R2D8 and C2D7 is input to pin 9 of OSD-IC IC212.
V-S signal, like the above, is output from pin 6 of inverter IC8A1 on PWB-MAIN, and input to pin 18 of OSD-IC IC212 via connector J212 on PWB-VIDEO from connector J103, and the signal with filters R2D6 and C2D6 is input to pin 16 of OSD-IC IC212. (D point)
OSD-IC IC212 detects the signal with this delay of 700ns (A and D points) and the position data (a to e mentioned below) of RGB OR signal (C point), and sends them to microcomputer IC101. The microcomputer IC101 calculates and processes the data to automatically adjust to ensure the appropriate width and position of screen.

- a: Drgbsta (AFC front edge + 700ns to Front edge of Picture)
- b: Drgbend (AFC front edge + 700ns to Back edge of Picture)
- c: Dvrgbsta (V_BLK front edge + 700ns to Front edge of Picture)
- d: Dvrgbend (V_BLK front edge + 700ns to Back edge of Picture)
- e: Dvsline (Number of vertical lines)

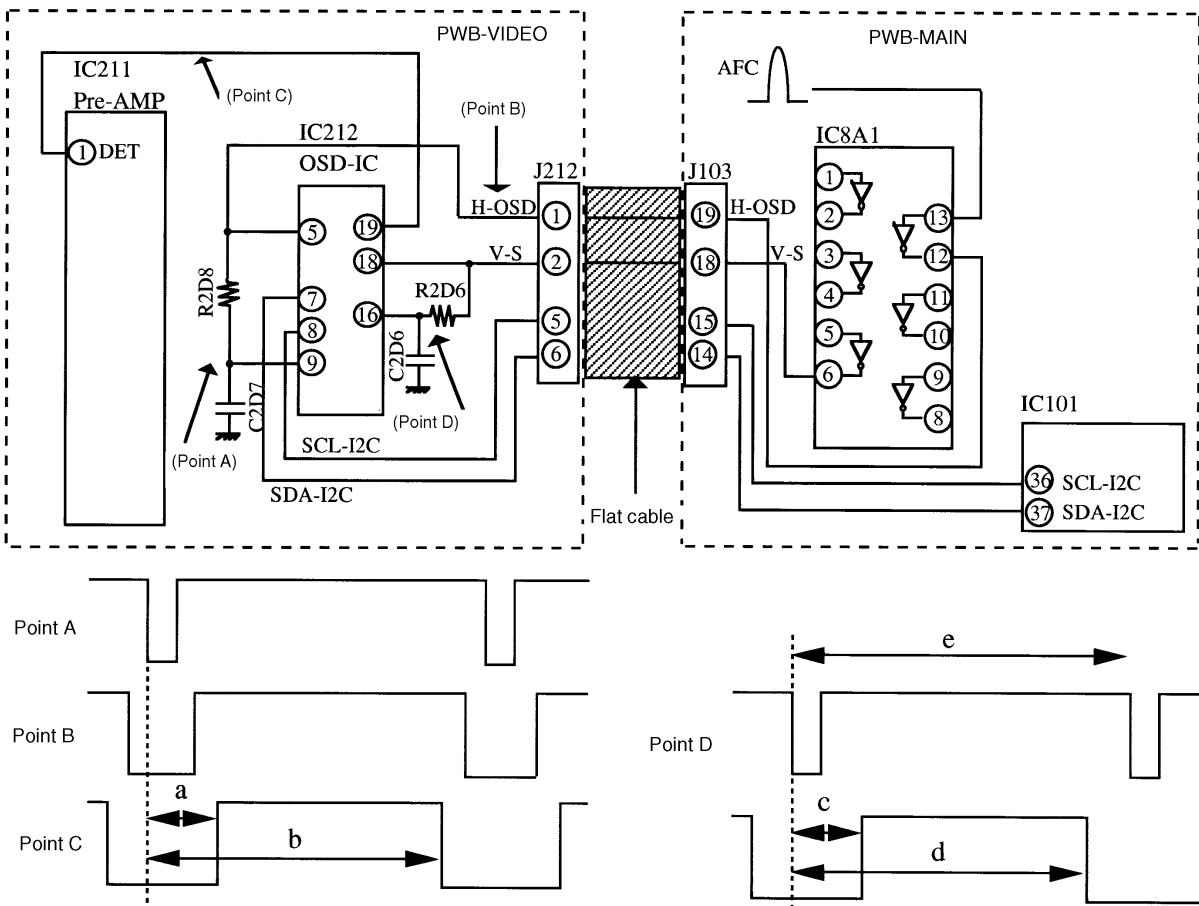


Figure 29 AUTO SIZE circuit

The diagram illustrates the internal architecture of the TMS320C42 video controller. Key components and their connections include:

- 6 CHANNELS PWM:** Receives PWMCLK and outputs PWM signals 0 through 5.
- PWM REGISTERS:** Receives MCLK and outputs PWM signals 0 through 5.
- DATA TRANSCEIVER MBUS:** Interfaces with the CPU (pins 7, 8) and the Display Memory/Control Registers (pins 8, 9, 9).
- BUS ARBITRATION LOGIC:** Receives MCLK and outputs Y (32) to the Row Buffer.
- VERTICAL CONTROL CIRCUIT:** Receives VFLB, CHS (8), VERD (6), and CH (6). It outputs MCLK and DHOR to the Horizontal Control and PLL.
- HORIZONTAL CONTROL and PLL:** Receives HBPOL and HPOL. It outputs HORD (7), PWM_CLK, and SC CCLK to other components.
- DISPLAY MEMORY and CONTROL REGISTERS:** Receives HORD, VERD, CH, OSD_EN, SHADOW, BSEN, and M1. It outputs M0, VPOL, HPOL, CLR, WADDR, WCOLOUR and CONTROL, and VM registers (73).
- ROW BUFFER:** Receives Y (32) and R (4). It outputs CCOLOURS and SELECT (13), CHS, and CWS.
- CHARACTER ROMS:** Receives CRADDR (8) and LP (4). It outputs CHAR (12 X 3).
- 12 BITS SHIFT X 3 REGISTERS:** Receives CWS and SHADOW. It outputs OSD_EN, LUMINANCE (3), and BLACKEDGE.
- COLOUR ENCODER:** Receives W (3), WCOLOUR and CONTROL (15), and CCOLOURS and SELECT (13). It outputs R (23), G (22), B (21), and FBKG (20).
- BACKGROUND & HATCH GENERATOR:** Receives WADDR (54) and outputs W (3).
- TIMING MEASUREMENT:** Receives HBPOL and HPOL. It outputs CTLPOL (8), TMCLK, M0, and M1.

Figure 30 IC212 (XC3825P2) block diagram

1.10 USB circuit

1.10.1 Outline

This monitor loads the standard USB SELF POWERED HUB with 1 upstream and 3 downstreams.

(1) Serial data bus

Data bus is connected from upstream connector J1A0 to upstream port of HUB controller IC1A0, and downstream connector J1A1 and J1A2 are connected from HUB controller. HUB controller relays data communication between the upstream side (PC) and the downstream side (device).

Downstream connection of HUB controller

Port on circuit diagram	Connector	Silk indication
port 1	J1A1	3
port 2	J1A2 (UP)	1
port 3	J1A2 (DOWN)	2

(2) Power supply to downstream

USB HUB of this monitor is SELF POWERED HUB, and it can supply the power of +5V 500mA (max) to each downstream from transformer T902 on PWB-MAIN. Further, HUB controller IC1A0 has the function of detecting overcurrent, and stops supplying the power to each downstream port when overcurrent (500mA or more) is detected at each port.

1.10.2 USB downstream power supply

(1) Supply of Vpp power

When HUB controller IC1A0 is recognized from the direction of upstream, the signal which functions as a switch of power output for a downstream port is output (IC1A0 #2, 16, 32). When IC1A0 #2, 16 and 32 become LOW, FET gates are turned ON, and EFT transistors Q1A1, Q1A2 and Q1A3 supply the power to the downstream ports (J1A1 #1, #5, J1A2 #1) respectively.

(2) Detection of overcurrent

HUB controller IC1A0 has the function of detecting overcurrent. If the current output at each port exceeds 550mA (min), gates of FET transistors Q1A1, Q1A2 and Q1A3 turn OFF (HIGH), automatically output of current stops only to the port that overcurrent is detected. In order to re-operate the port that overcurrent is detected, either of the followings should be carried out:

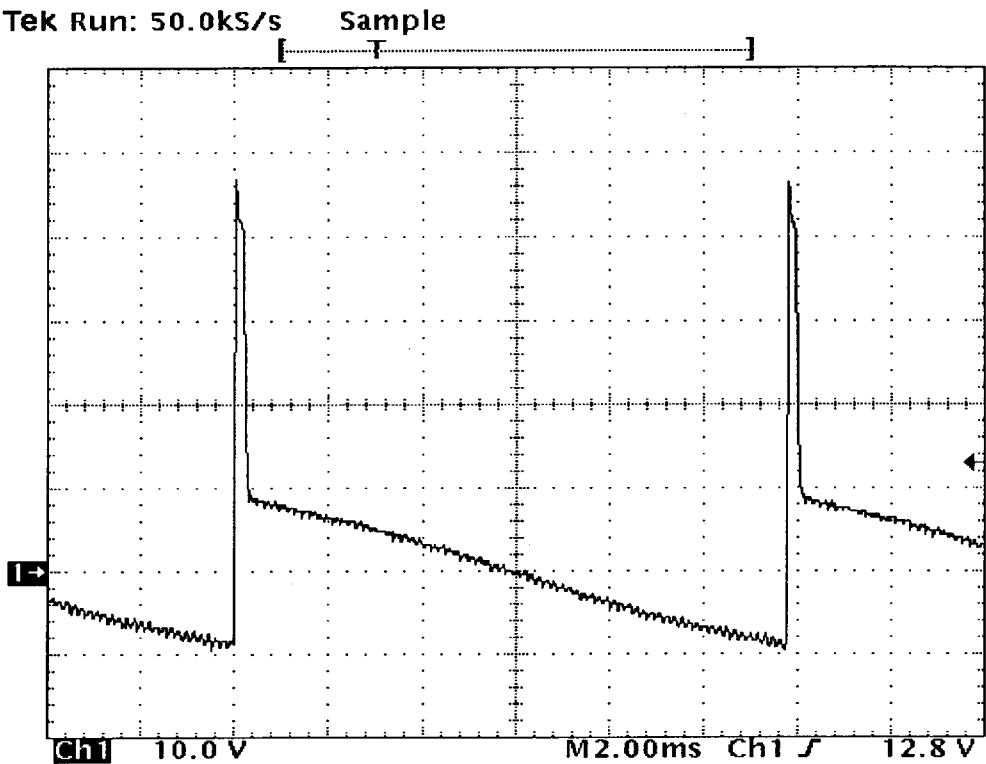
1. OFF/ON of monitor power supply
2. Pulling-out and pulling-in of upstream cable
3. Restart of PC

1.10.3 HUB controller power output

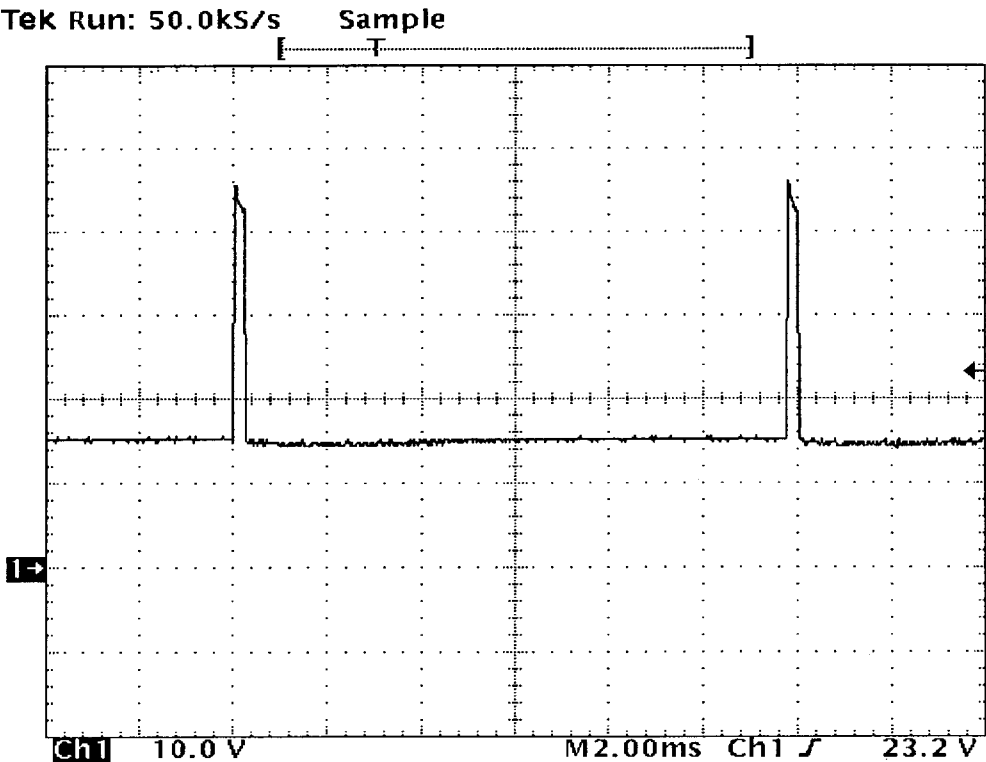
HUB controller IC1A0 has a built-in 3.3V regulator, and outputs from IC1A0 #1.

1.11 Wave form of main circuit voltage

1.IC401 #2

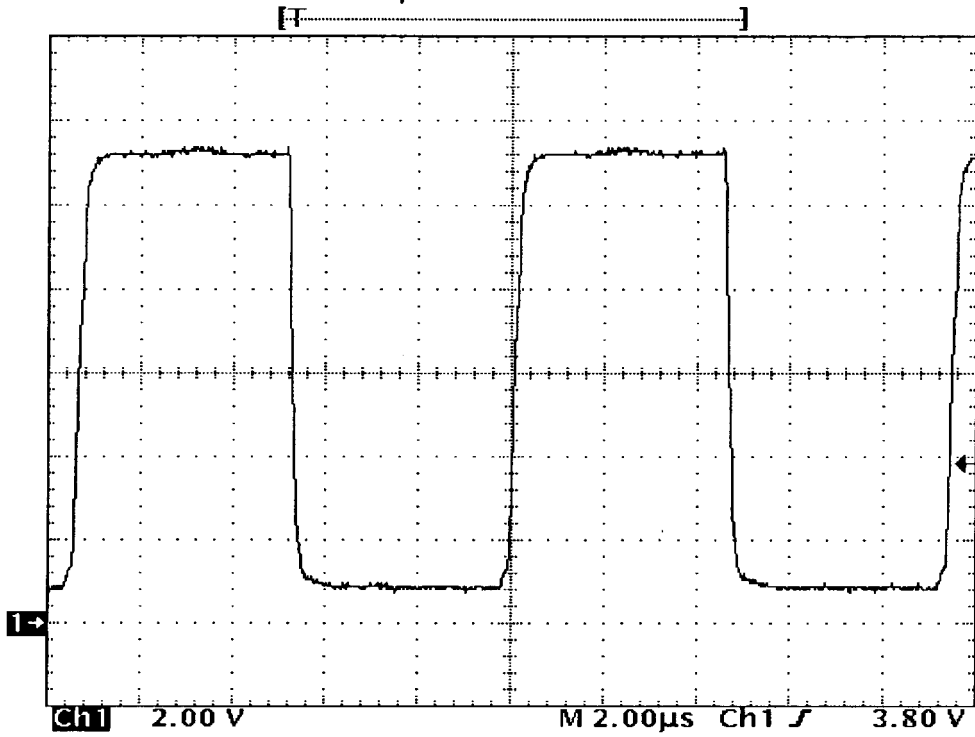


2.IC401 #3



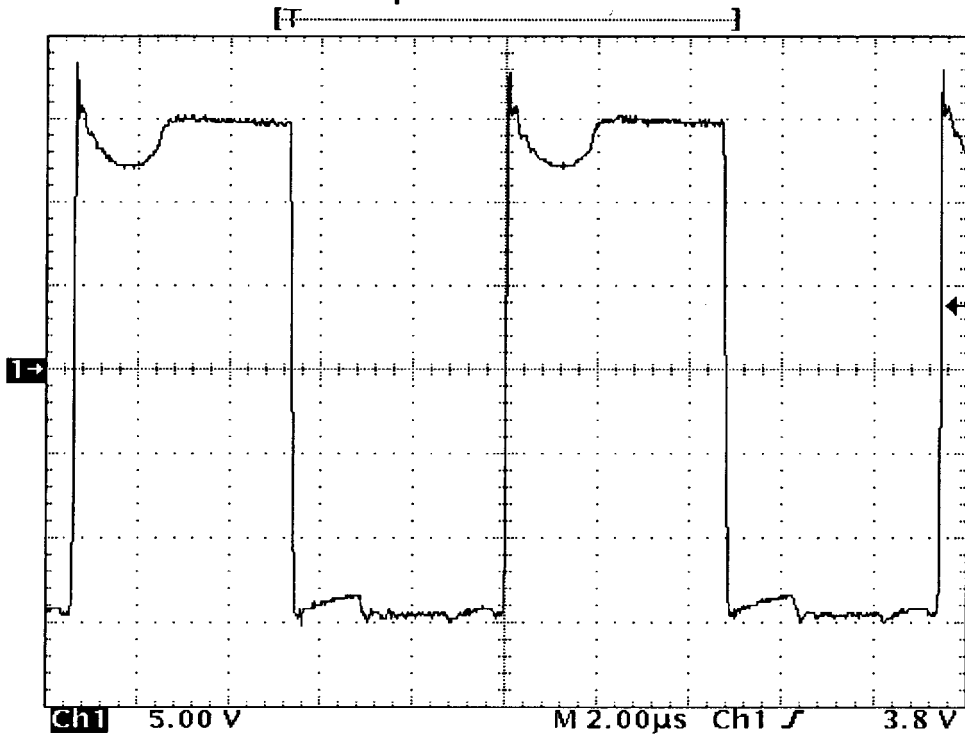
3.Q561 #E

Tek Run: 50.0MS/s Sample

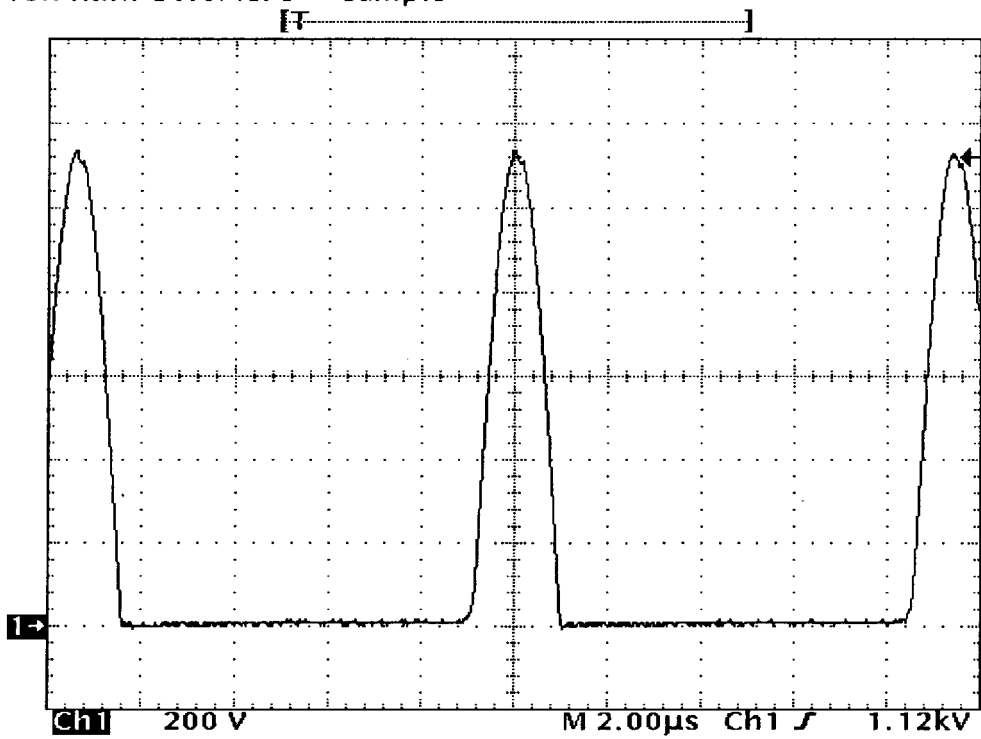


4.T501 #1

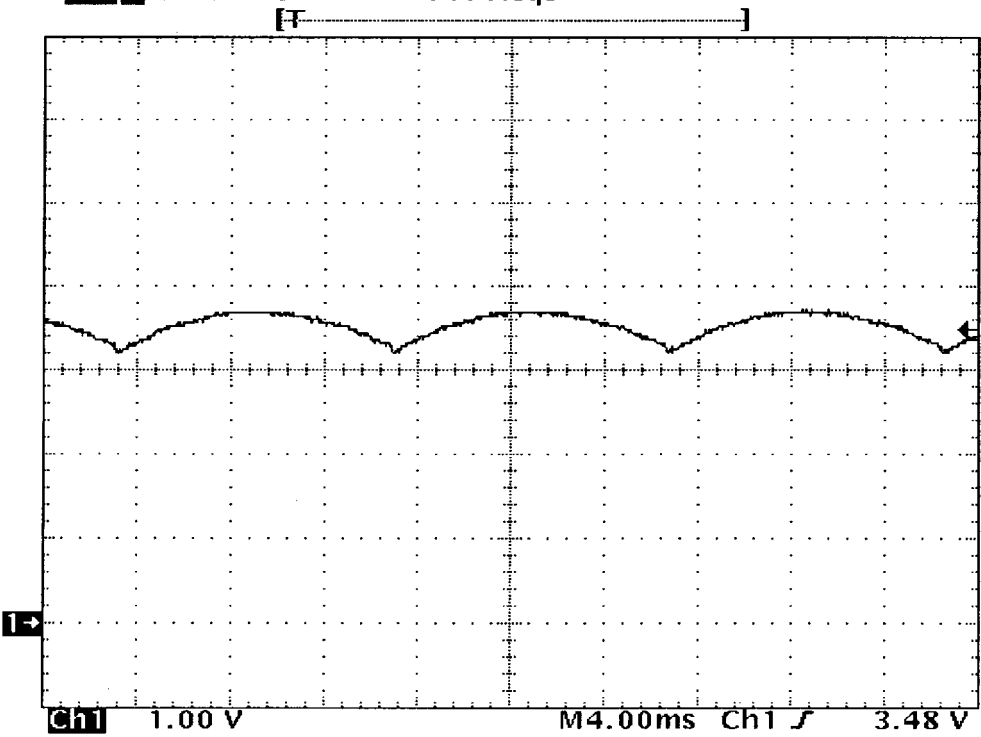
Tek Run: 50.0MS/s Sample



Tek Run: 50.0MS/s Sample



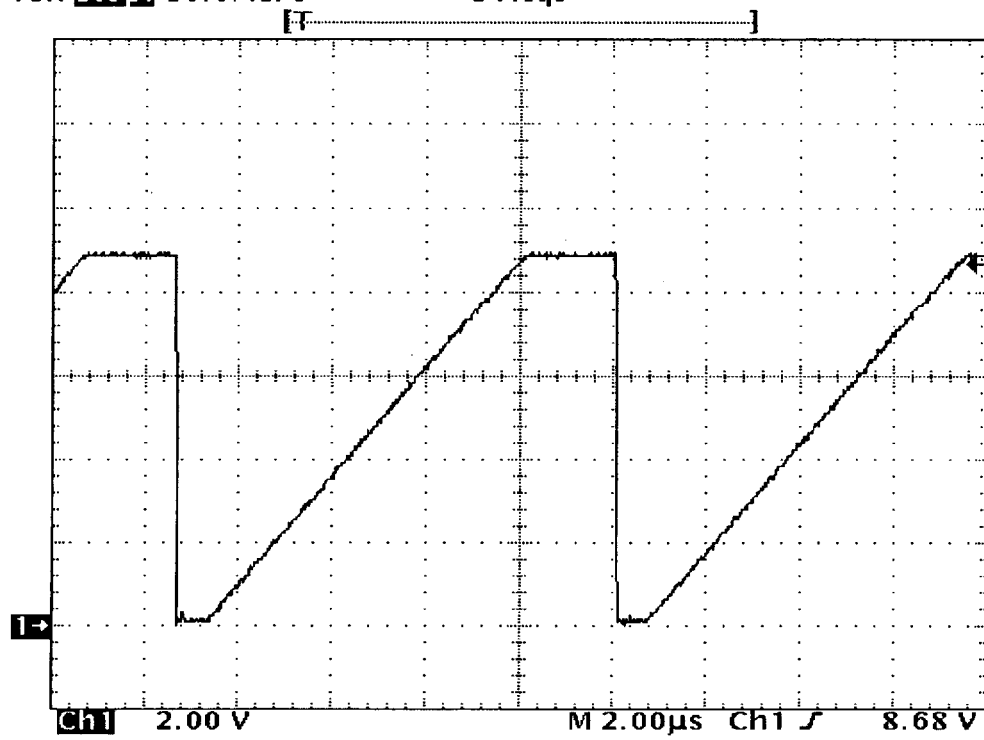
Tek Stop: 25.0kS/s 141 Acqs



7. IC5J1 #3

Tek **Stop:** 50.0MS/s

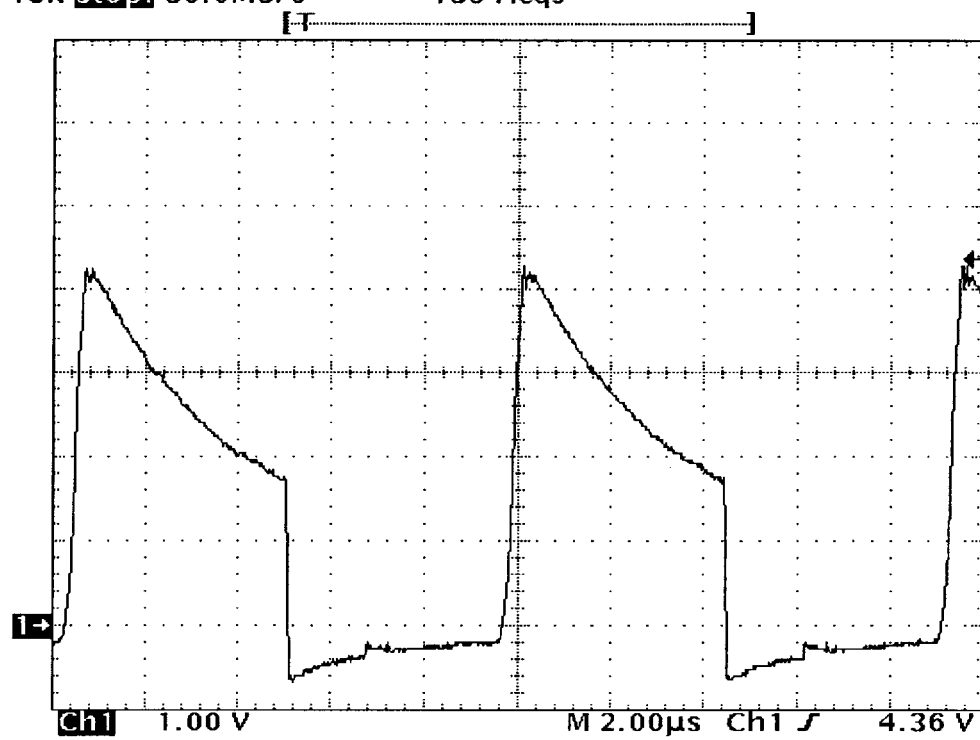
8 Acqs



8. IC5J1 #8

Tek **Stop:** 50.0MS/s

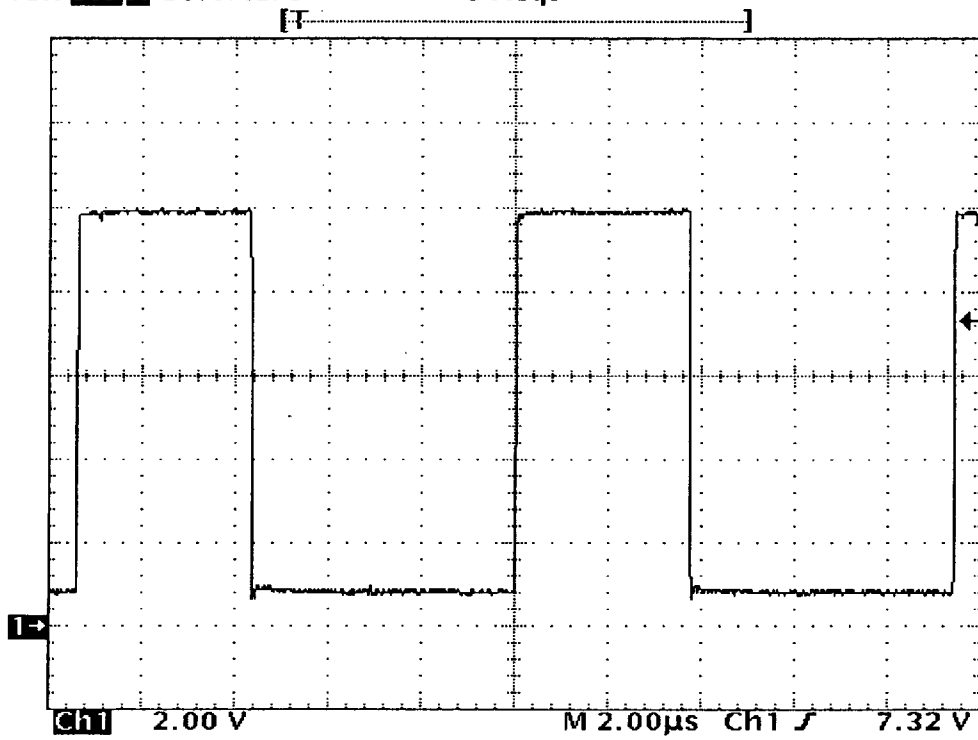
139 Acqs



9.1C5J1 #9

Tek **Stop:** 50.0MS/s

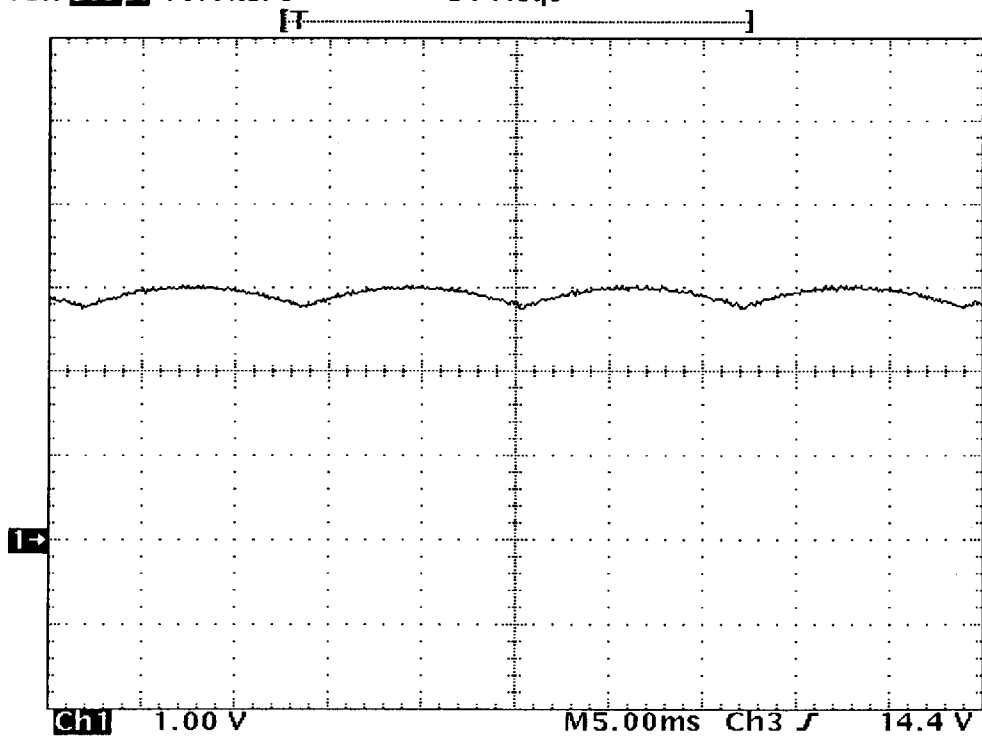
8 Acqs



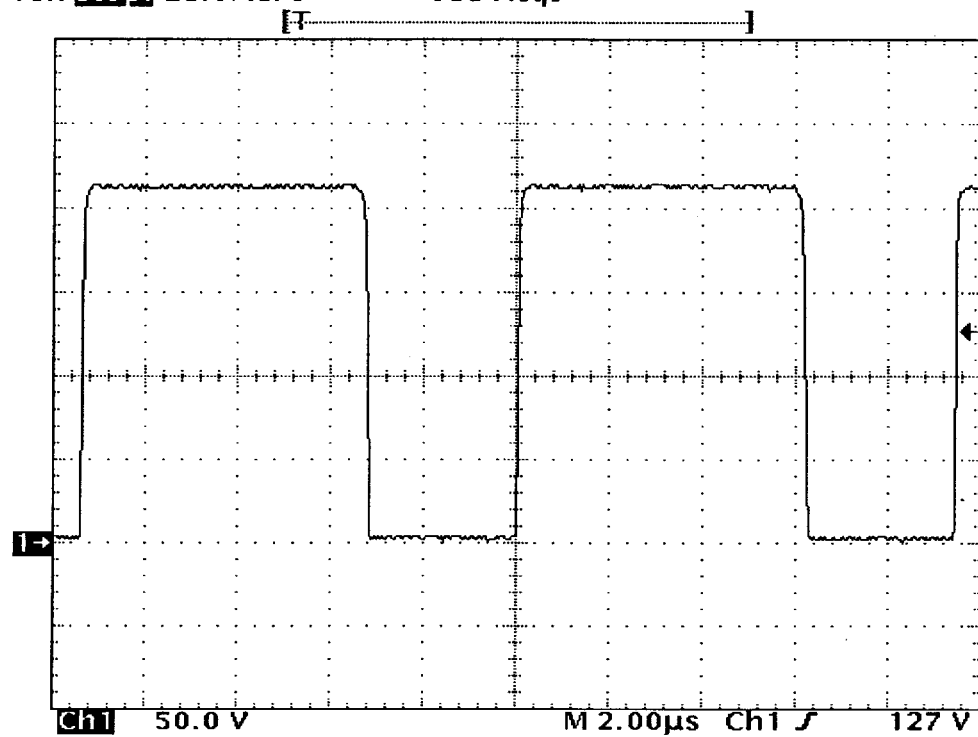
10.R5J1-R5J2

Tek **Stop:** 10.0kS/s

31 Acqs



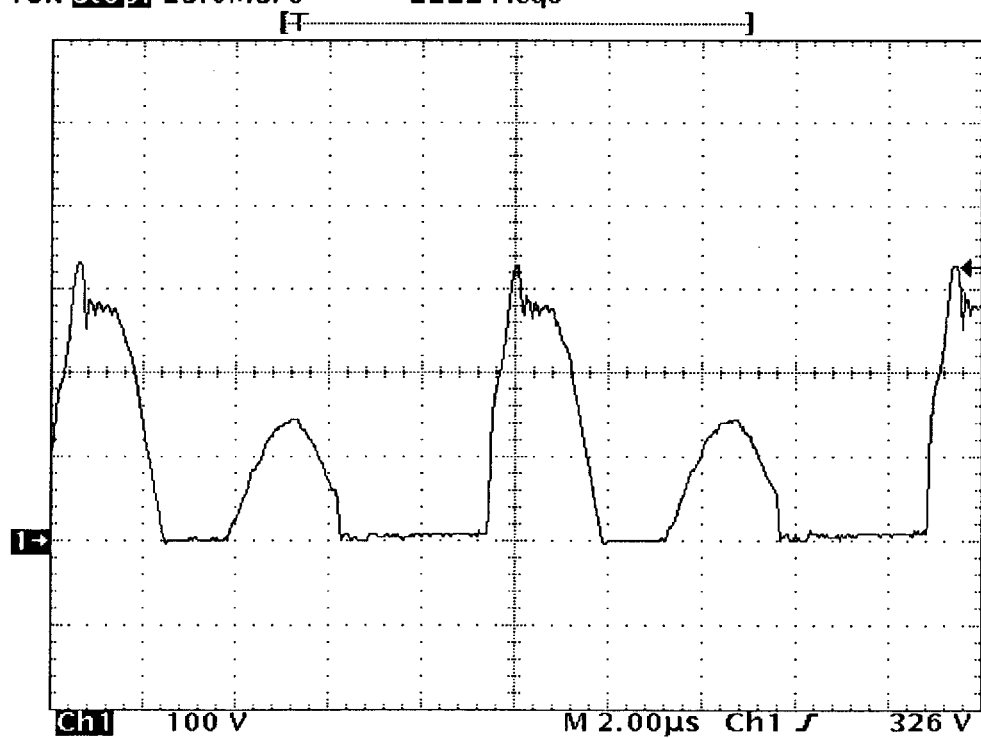
655 Acqs



12.T701 #1

Tek Stop: 25.0MS/s

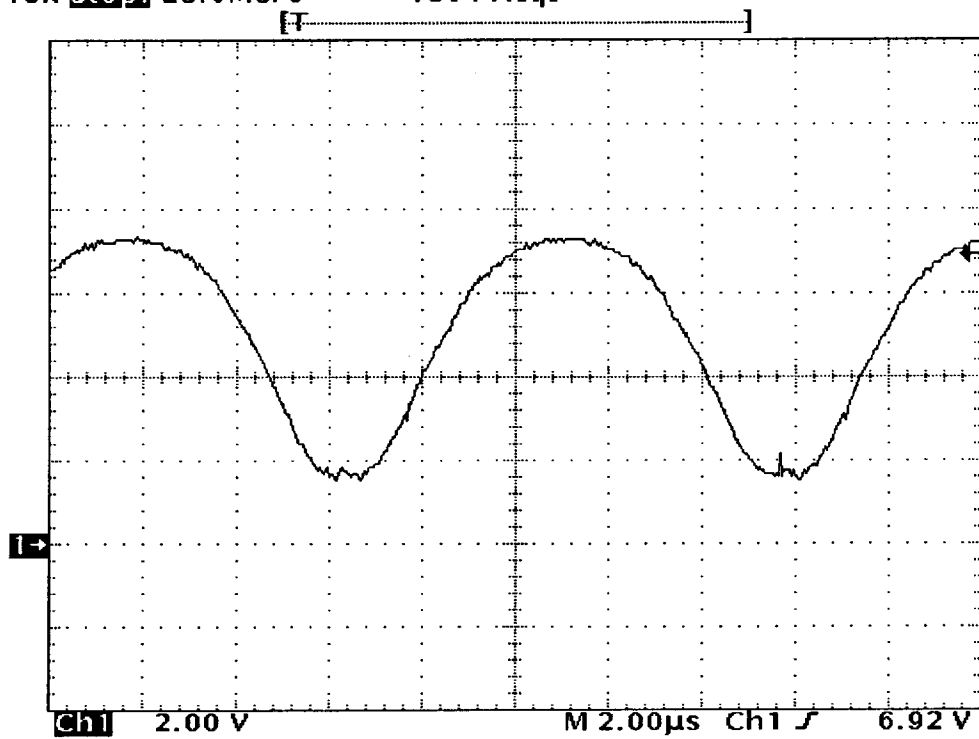
2222 Acqs



13.Q7B5 #B

Tek **Stop** 25.0MS/s

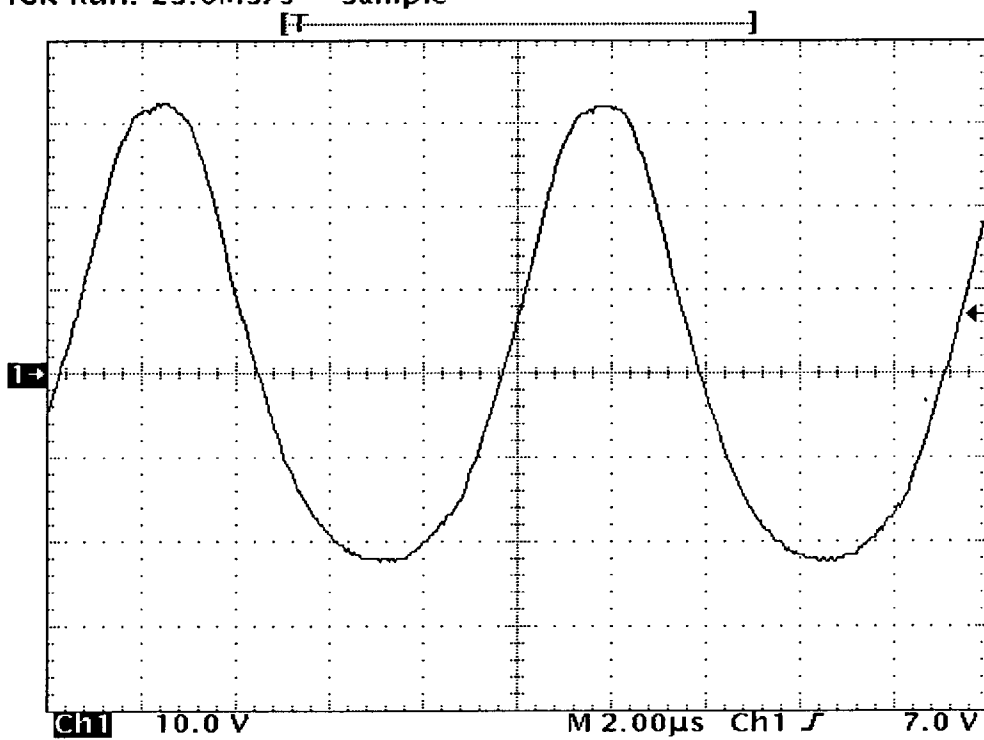
1504 Acqs



14.T7A1 #3

Tek Run: 25.0MS/s

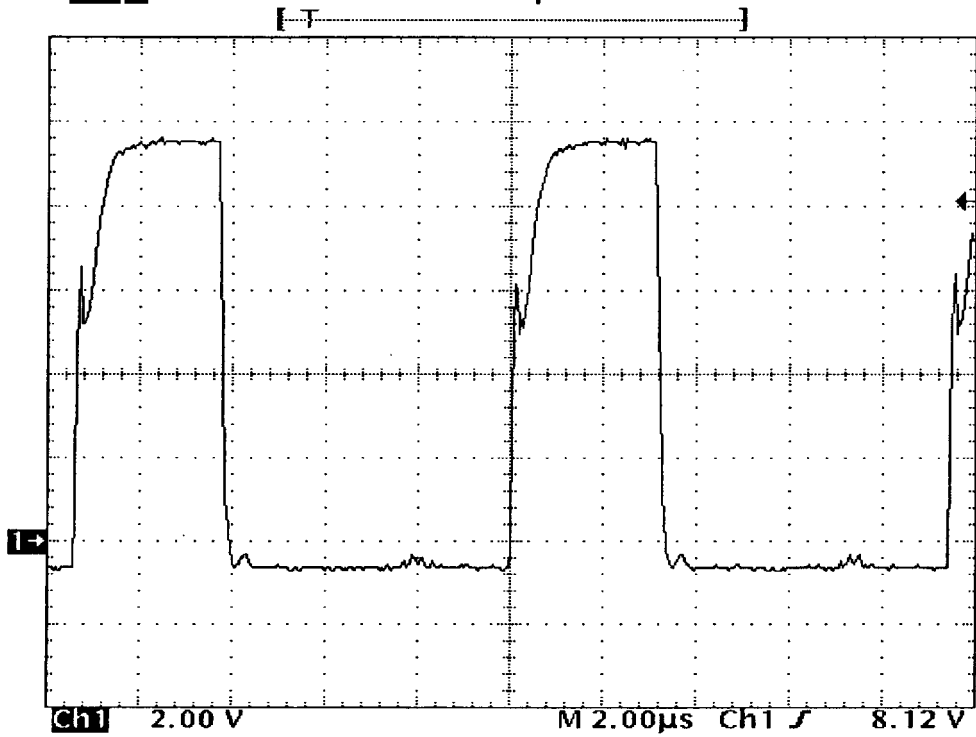
Sample



15.Q701 #G

Tek Stop: 25.0MS/s

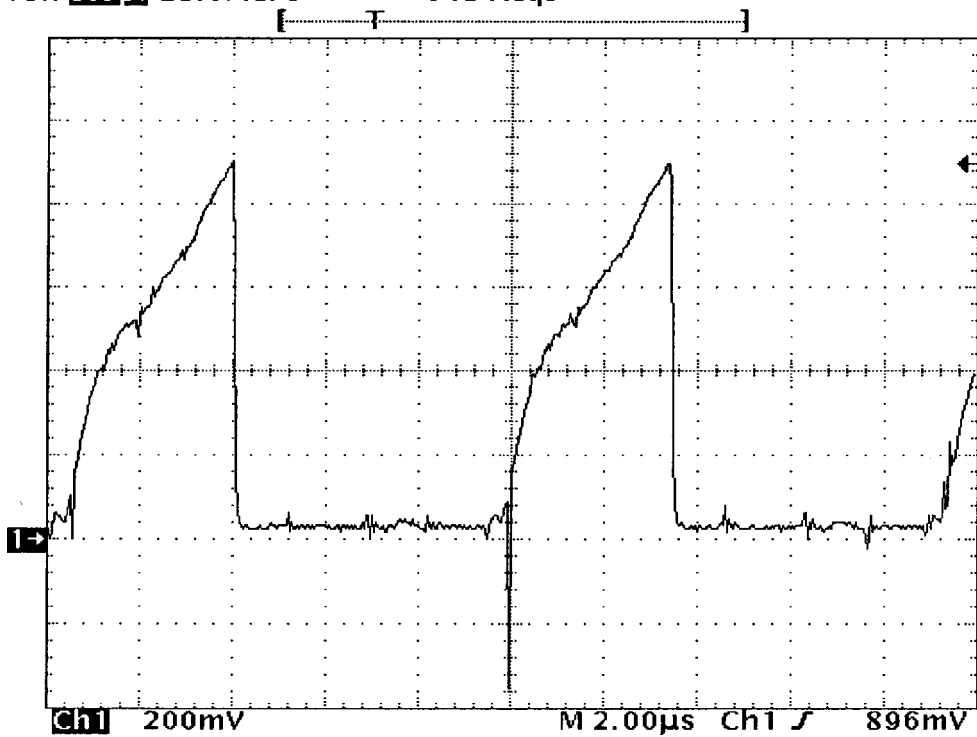
13 Acqs



16.IC701 #4

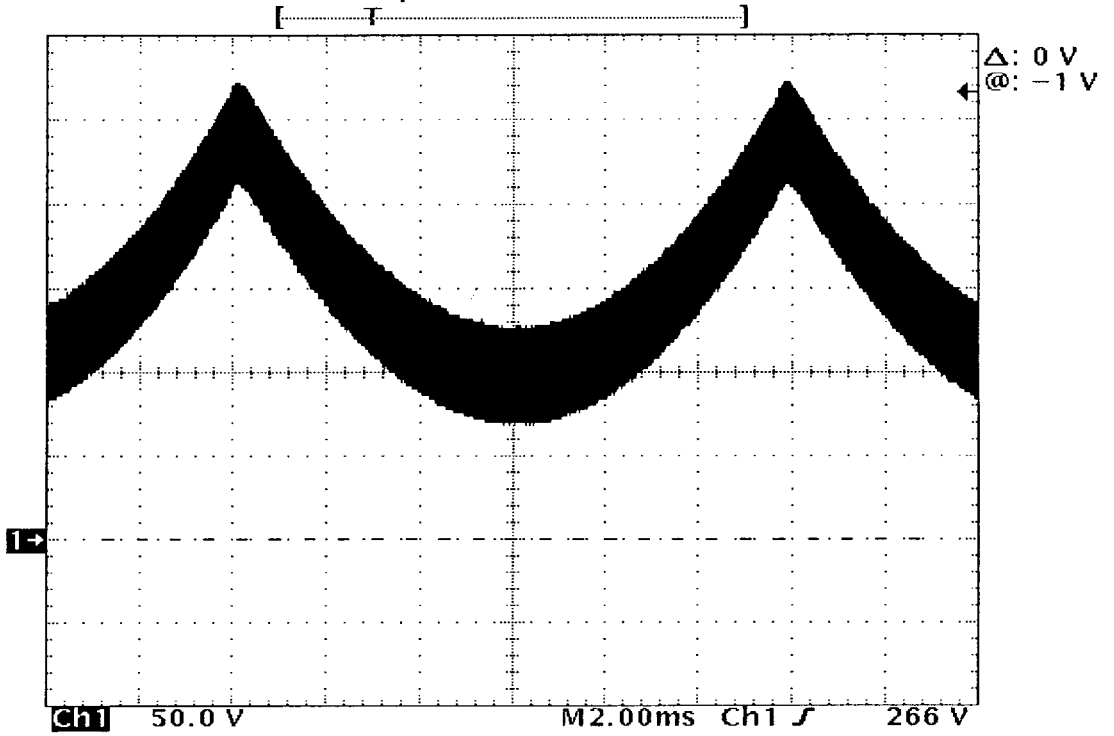
Tek Stop: 25.0MS/s

645 Acqs



17.T7A1 #8

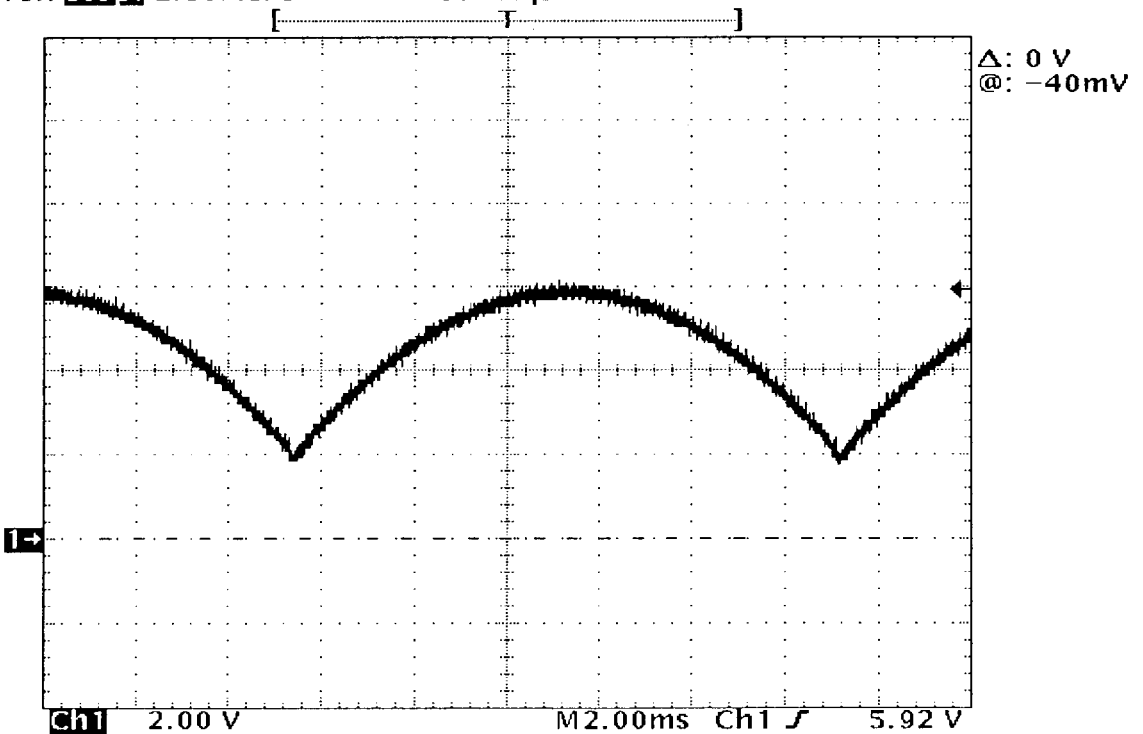
Tek Run: 2.50MS/s Sample



18.Q7A1 #B

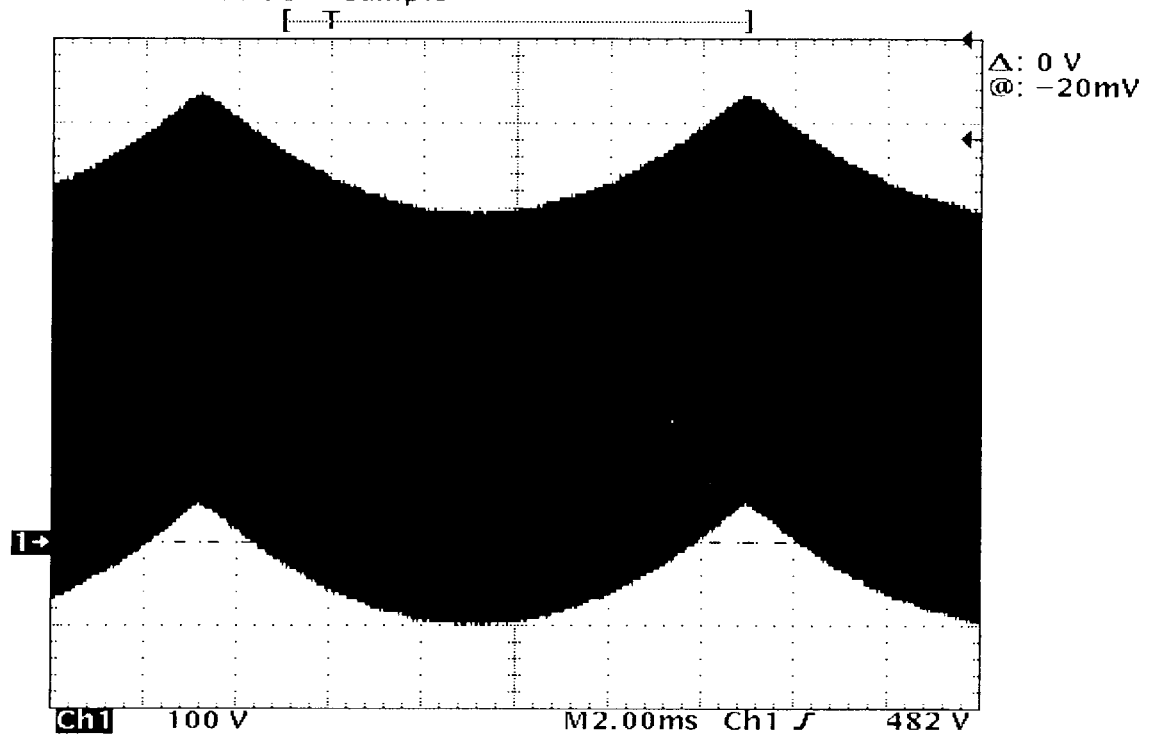
Tek Stop: 2.50MS/s

97 Acqs



19.T701 #12

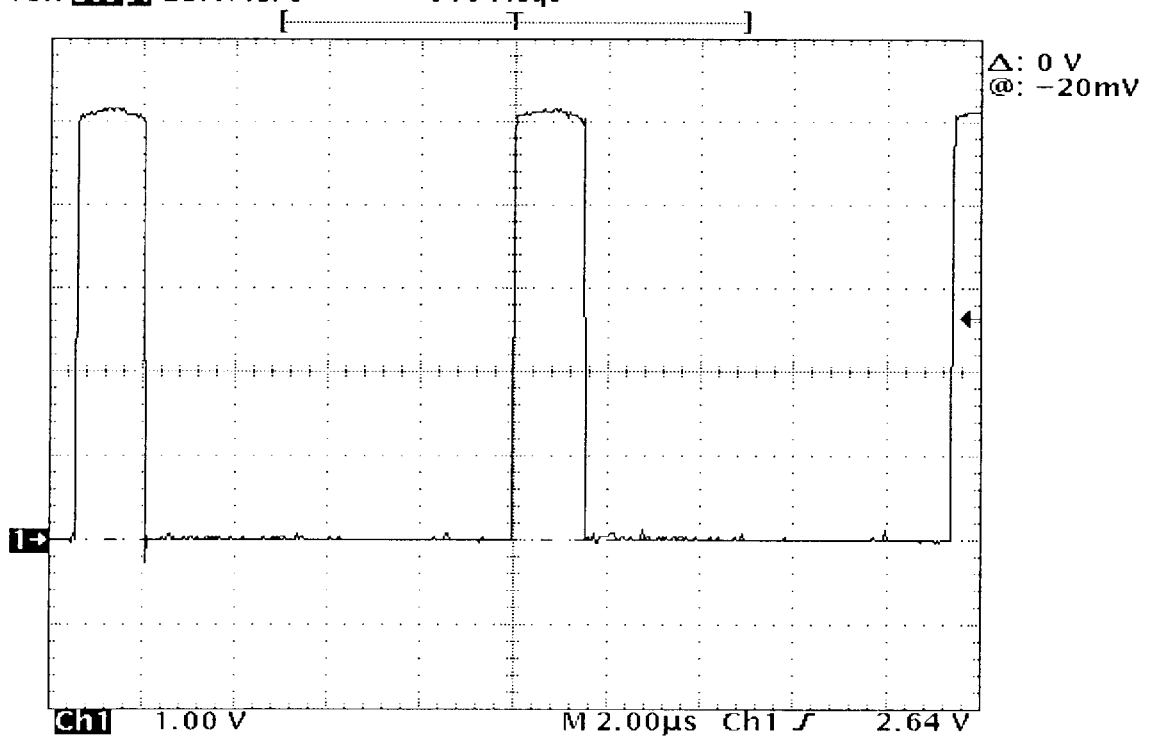
Tek Run: 2.50MS/s Sample



20.J601 #10 AFC

Tek Stop: 25.0MS/s

616 Acqs

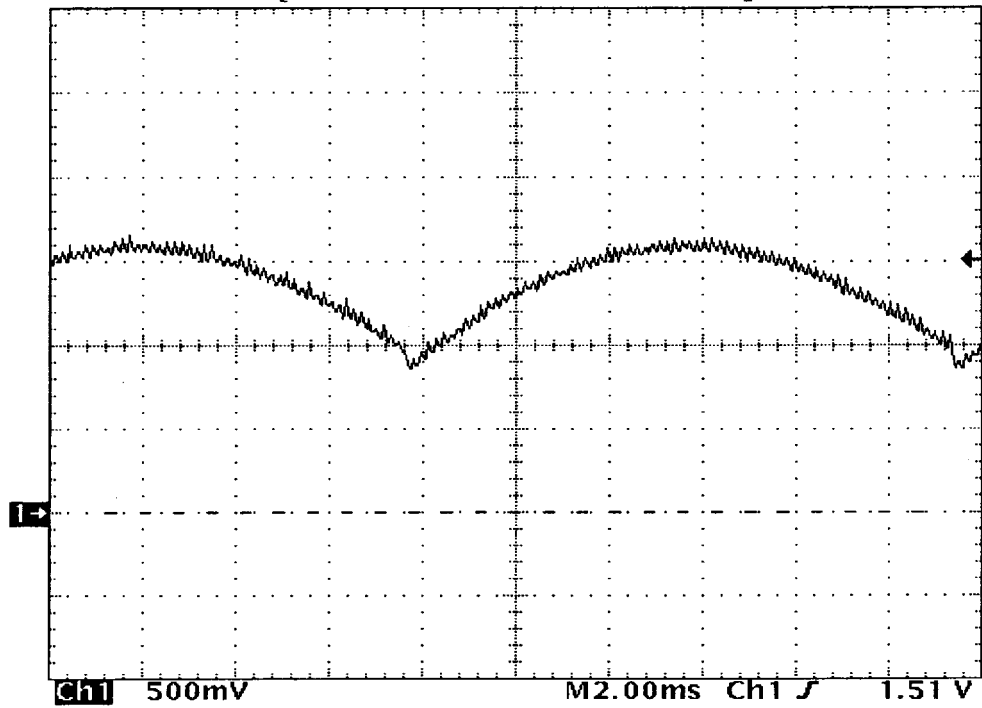


21.J600 #12 EW

Tek Stop: 25.0kS/s

5 Acqs

Δ: 0 V
@: -10mV

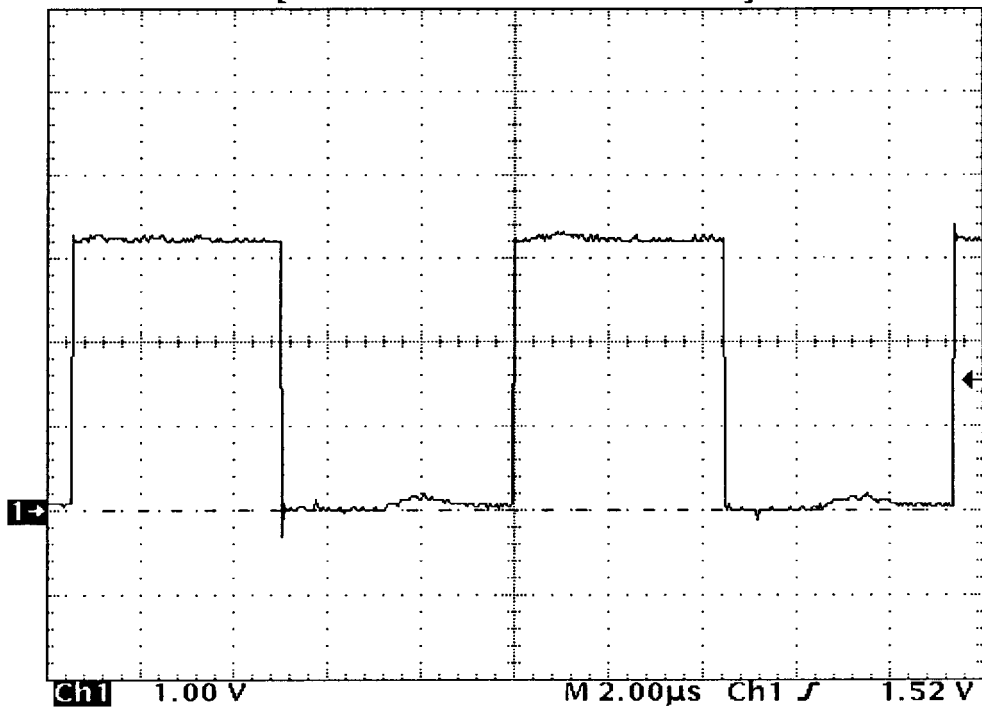


22.J601 #11 HD

Tek Stop: 25.0MS/s

381 Acqs

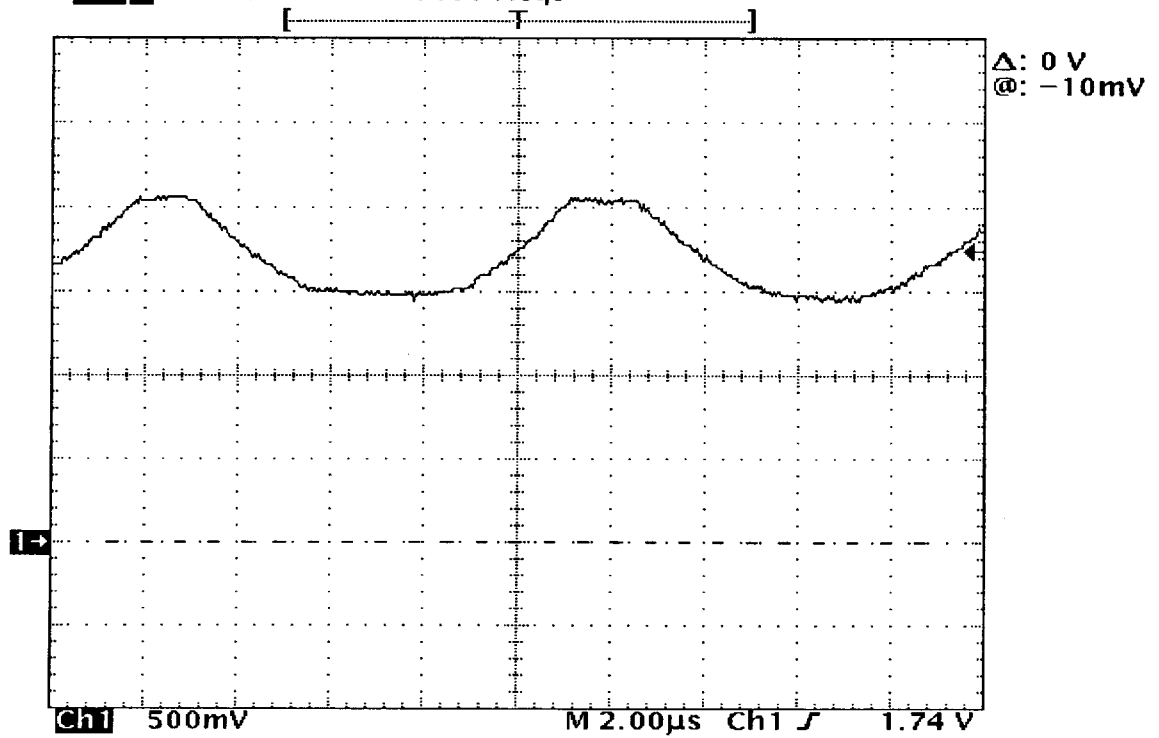
Δ: 0 V
@: -20mV



23.J600 #6 HDF

Tek **Stop:** 25.0MS/s

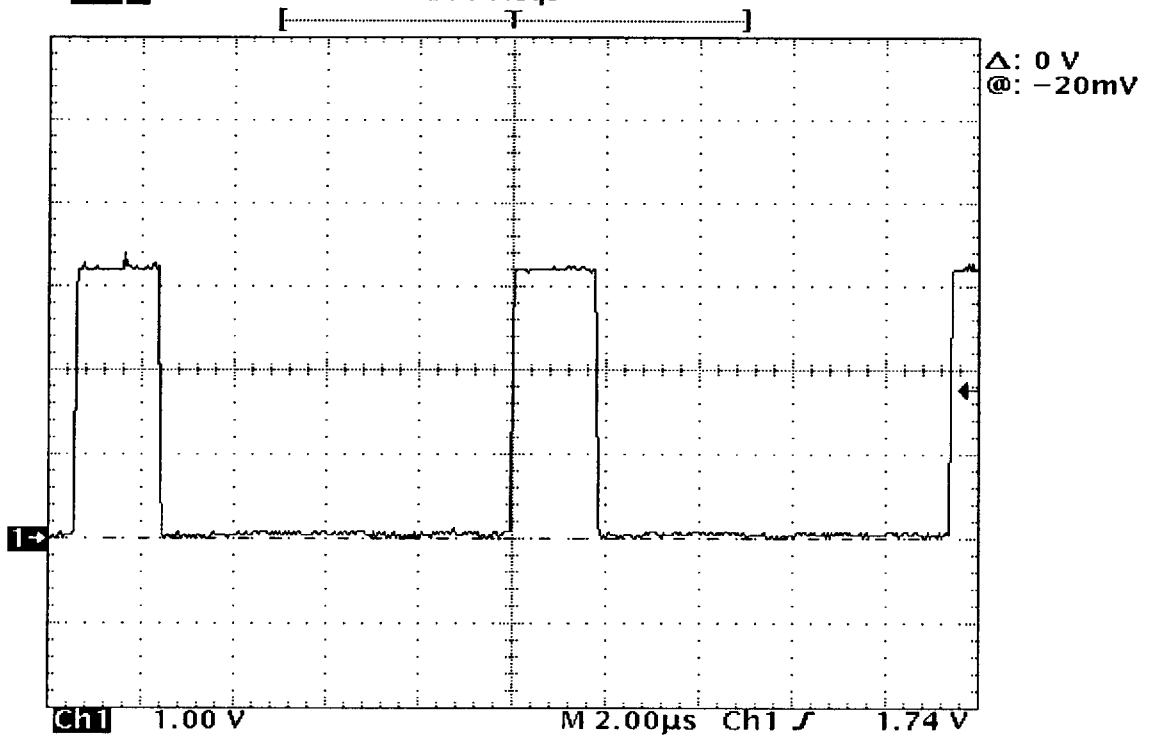
1406 Acqs



24.J600 #1 HV-BLK

Tek **Stop:** 25.0MS/s

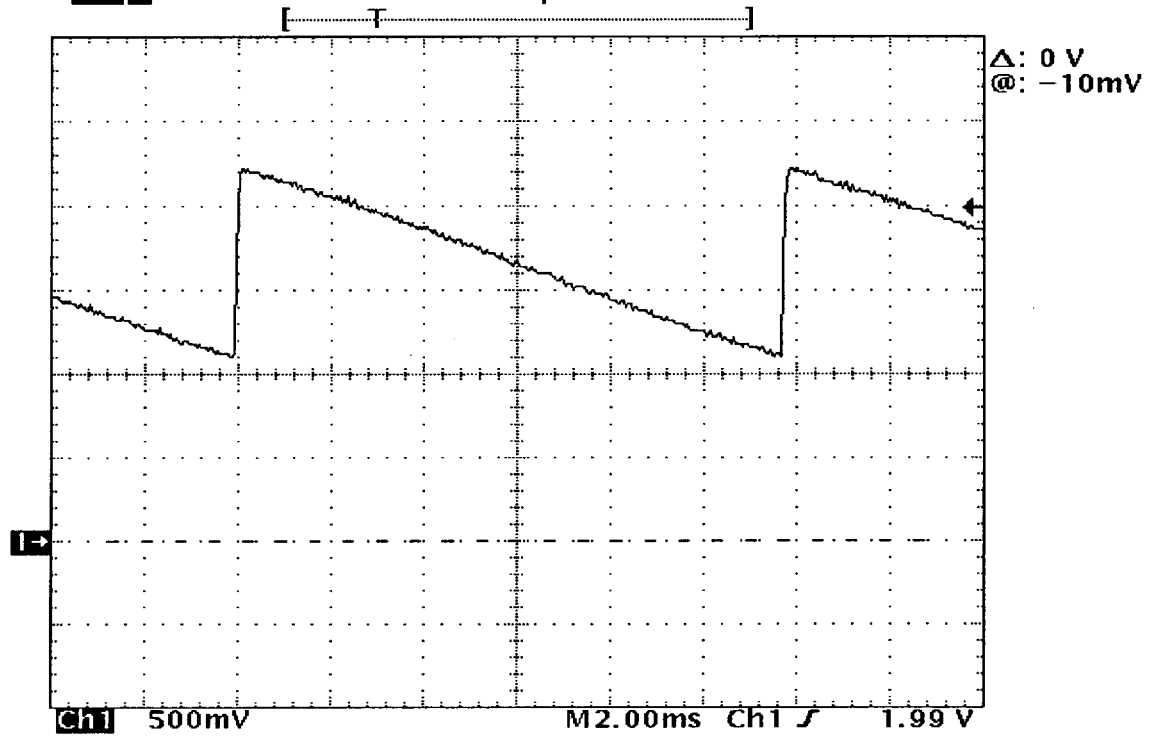
366 Acqs



25.J600 #15 V-SAW

Tek **Stop:** 25.0kS/s

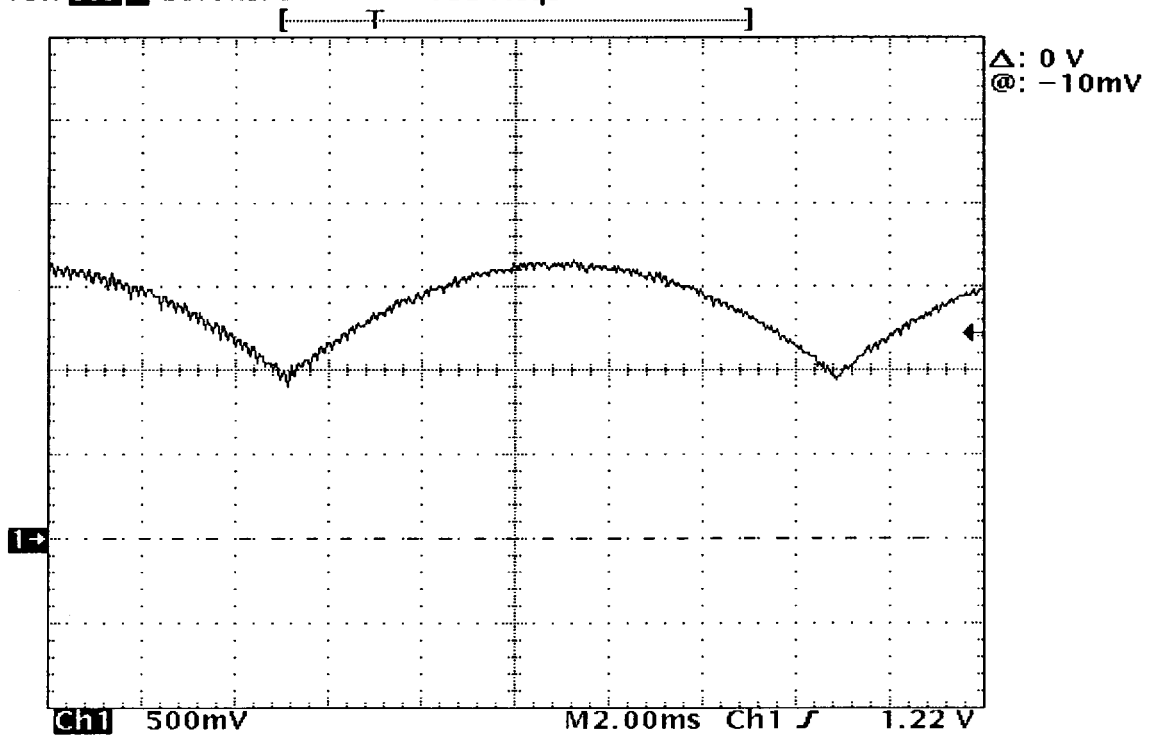
149 Acqs



26.J600 #4 VDF

Tek **Stop:** 25.0kS/s

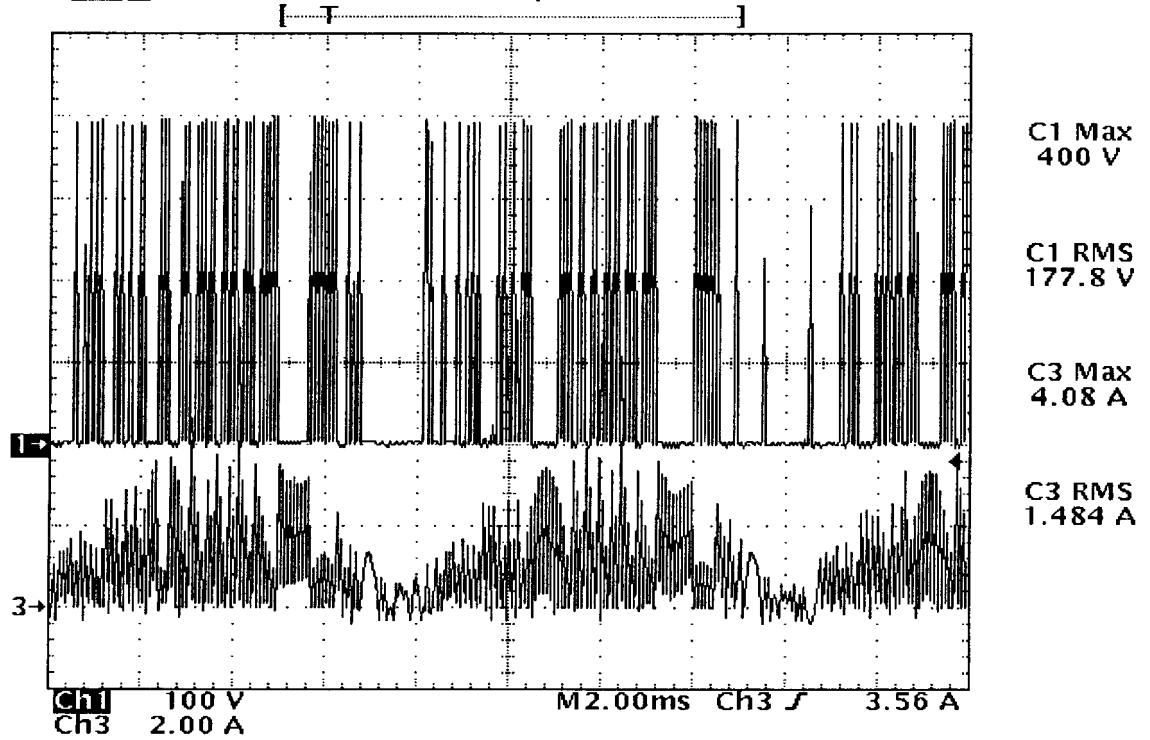
185 Acqs



27.Q901 Vds,Id

Tek **Stop:** 25.0kS/s

19 Acqs



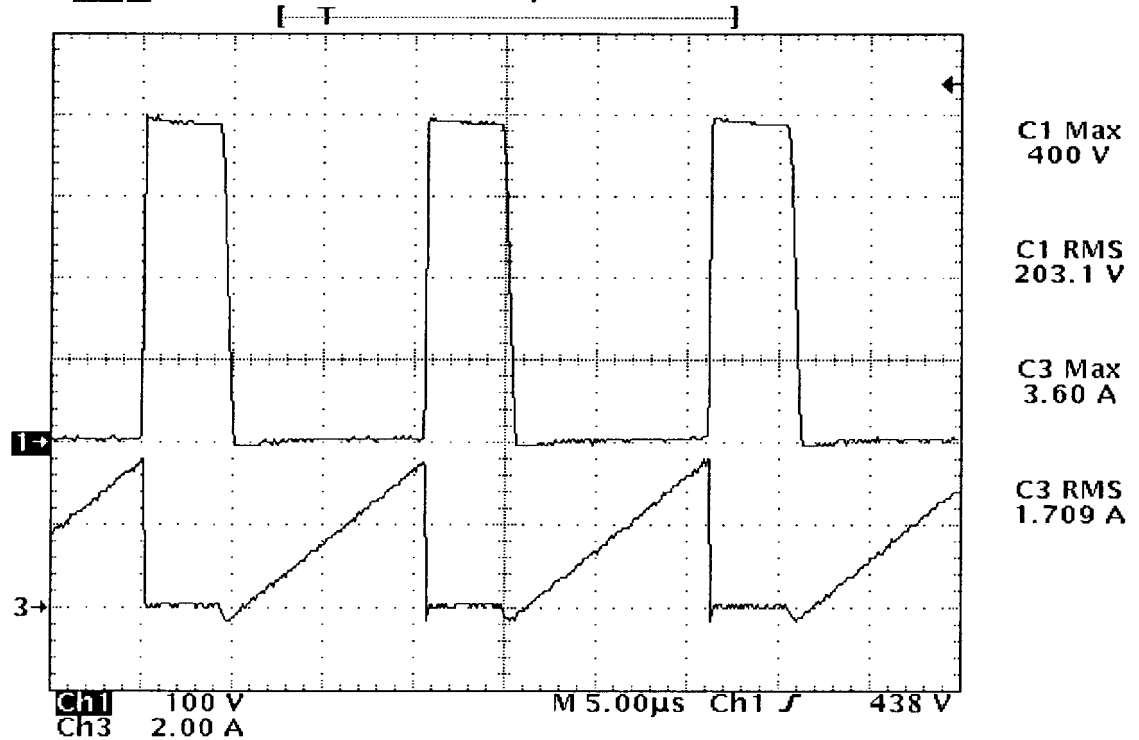
Top: Q901 Vds

Bottom: Q901 Id

28.IC902 Vds,Id(enlarged)

Tek **Stop:** 10.0MS/s

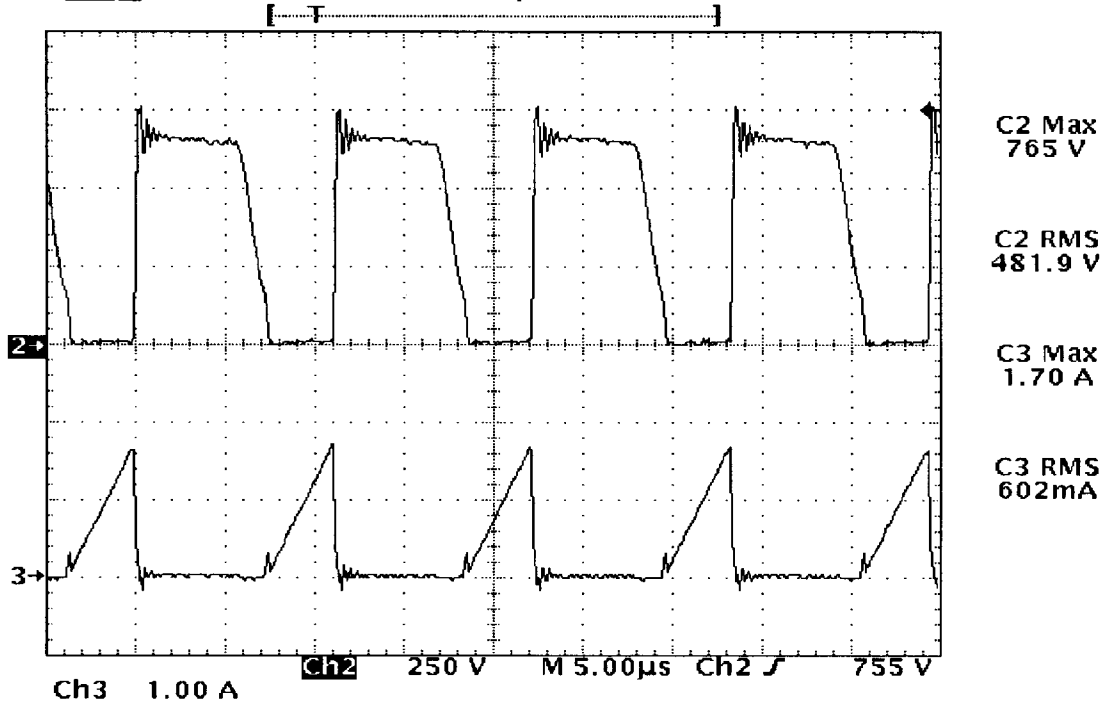
17 Acqs



29.IC902 Vds,Id

Tek **Stop:** 10.0MS/s

127 Acqs



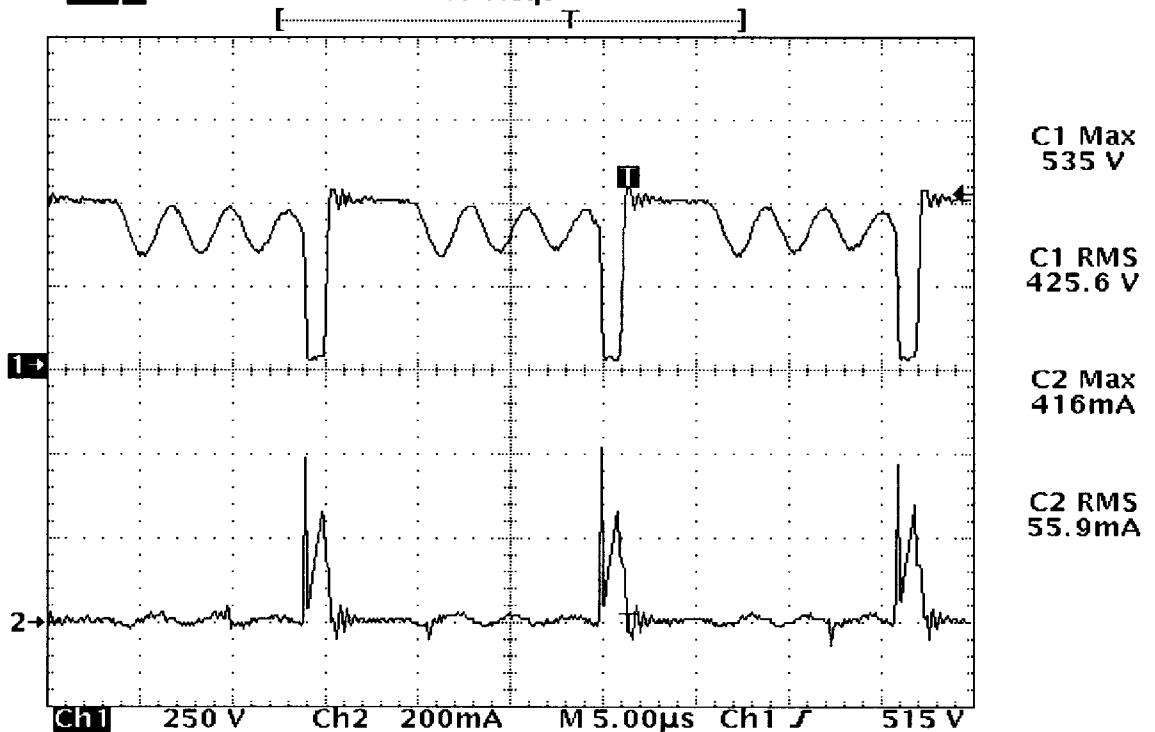
Top: IC902 Vds

Bottom: IC902 Id

30.IC903 Vds,Id

Tek **Stop:** 10.0MS/s

17 Acqs



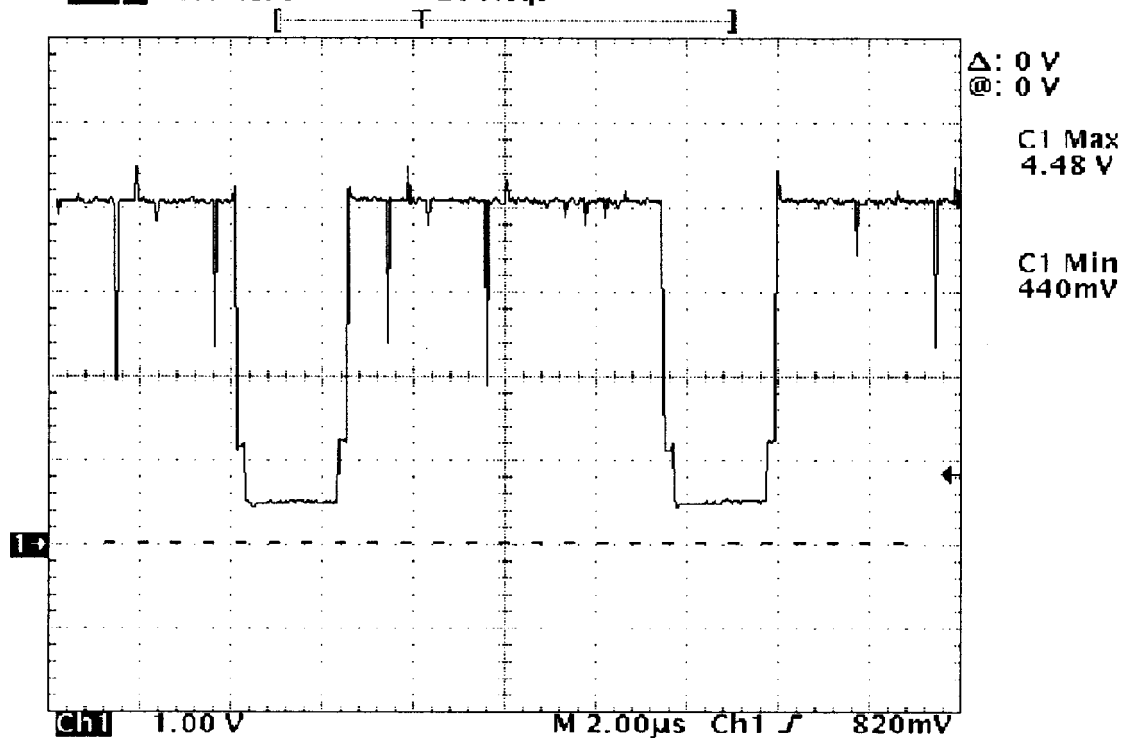
Top: IC903 Vds

Bottom: IC903 Id

31.VIDEO-IN

Tek **Stop:** 25.0MS/s

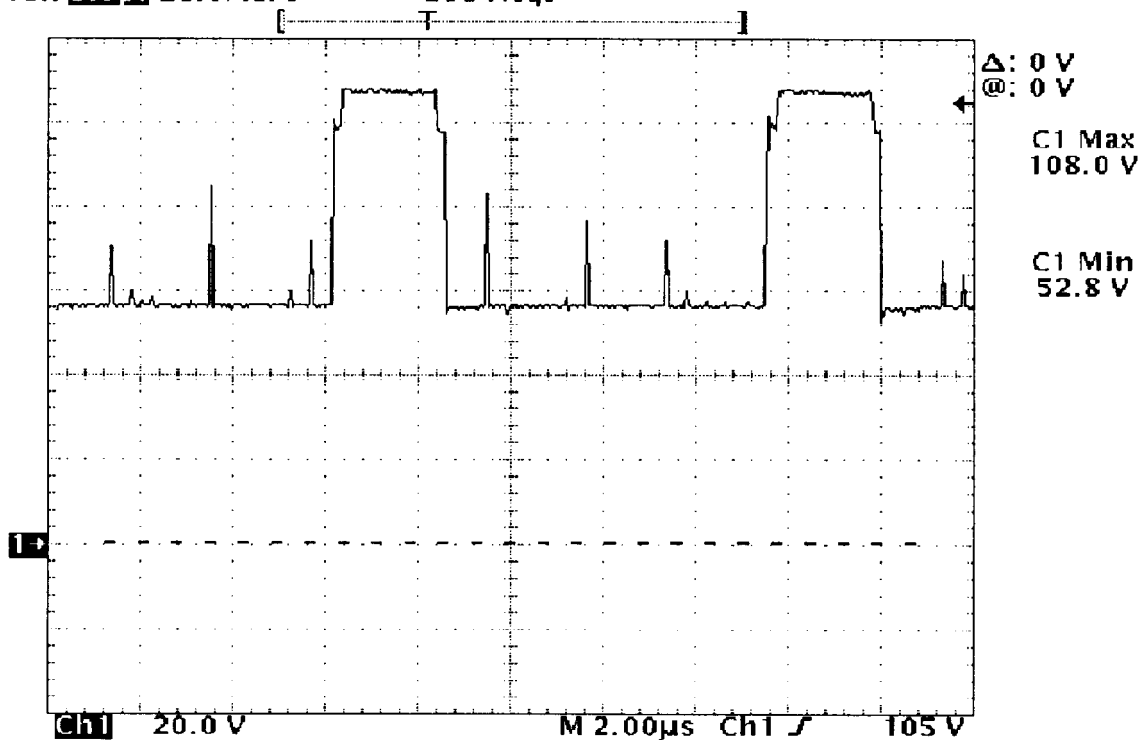
26 Acqs



32.VIDEO-OUT

Tek **Stop:** 25.0MS/s

253 Acqs



253 Acqs

